

High-Performance Vertical Organic Electrochemical Transistors

Mary J. Donahue, Adam Williamson, Xenofon Strakosas, Jacob T. Friedlein, Robert R. McLeod, Helena Gleskova,* and George G. Malliaras*

Organic electrochemical transistors (OECTs) are promising transducers for biointerfacing due to their high transconductance, biocompatibility, and availability in a variety of form factors. Most OECTs reported to date, however, utilize rather large channels, limiting the transistor performance and resulting in a low transistor density. This is typically a consequence of limitations associated with traditional fabrication methods and with 2D substrates. Here, the fabrication and characterization of OECTs with vertically stacked contacts, which overcome these limitations, is reported. The resulting vertical transistors exhibit a reduced footprint, increased intrinsic transconductance of up to 57 mS, and a geometry-normalized transconductance of 814 S m⁻¹. The fabrication process is straightforward and compatible with sensitive organic materials, and allows exceptional control over the transistor channel length. This novel 3D fabrication method is particularly suited for applications where high density is needed, such as in implantable devices.


Since the initial demonstration of a working transistor in 1947, reduction in physical size (downscaling or miniaturization) of various inorganic transistors has led to better utilization of available substrate space while improving transistor performance and lowering power requirements and device cost.^[1]

Dr. M. J. Donahue, Dr. X. Strakosas, Prof. G. G. Malliaras^[†]
Department of Bioelectronics
Ecole Nationale Supérieure des Mines
CMP-EMSE, MOC, 880 route de Mimet, 13541 Gardanne, France
E-mail: gm603@ca.ac.uk

Dr. A. Williamson
Inserm
UMR INSERM
1106, 13005 Marseille, France

Dr. J. T. Friedlein, Prof. R. R. McLeod
Department of Electrical, Computer, and Energy Engineering
University of Colorado
Boulder, CO 80309-0425, USA

Dr. H. Gleskova
Department of Electronic and Electrical Engineering
University of Strathclyde
Glasgow, G1 1XW, UK
E-mail: helena.gleskova@strath.ac.uk

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/adma.201705031>.

^[†]Present address: Electrical Engineering Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, UK

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Downscaling of transistors has enabled the advancement of a wide range of commonly used electronic devices.^[2] Compared to traditional inorganic transistors, the development of transistors based on organic materials is at a relatively young phase. Downscaling of organic field-effect transistors (OFETs) has been primarily driven by active-matrix display technologies,^[3] with much effort focused on understanding and optimizing organic semiconductor (OSC) morphology and charge transport properties.^[4] An alternative organic transistor structure to the OFET, the organic electrochemical transistor (OECT), has also benefitted from OSC materials research, progressing significantly in the last decade. Whereas OFET current modulation relies on the field-effect, responding to charge accu-

mulation at the dielectric interface of the channel, the current in OECTs is controlled by the injection of ions from an electrolyte into the bulk of the channel. This makes them particularly suitable for biointerfacing applications where documented advantages of organic technologies are numerous.^[5,6] Examples include neural implants,^[7-14] in vitro arrays for biological assays,^[15-21] and neuromorphic devices.^[22-25] OECTs have reached a significant level of maturity and a major contemporary challenge is to pursue miniaturization for increasing density and improving performance.

Various vertical transistor orientations have been previously investigated in OFETs.^[26-30] However, the majority of these devices suffer from low mobilities, undesired leakage currents, and rather high driving voltages. By contrast, OECTs are inherently suitable for miniaturization. This results from the different principle of OECT operation, good-quality contacts to the channel due to the high levels of doping, and simplicity of the fabrication process. A first attempt to make use of a vertical architecture in combination with poly(3,4-ethylenedioxythiophene) doped with poly(styrenesulfonate) (PEDOT:PSS) deals with screen printed devices. Vertical vias in plastic or paper are exploited to make use of both sides of the substrate.^[31] Here, we demonstrate vertical organic electrochemical transistors (vOECTs) with PEDOT:PSS channels, fabricated using photolithography. The fabrication process takes advantage of the unique ionic-to-electronic transducing capability of the OECT, while maintaining low-voltage operation, compatibility with flexible substrates, and amplification

with high signal-to-noise ratio. For biointerfacing applications this provides a means to considerably increase the number of possible recording sites (transistor density) while significantly improving transistor performance. Indeed, the geometry-normalized intrinsic transconductance shown here reaches values greater than 800 S m^{-1} , the highest reported for OECTs to date.^[32]

The vOECT fabrication process is interesting because it does not require exotic methods. It relies on a sacrificial layer lithography process described previously^[32] to pattern PEDOT:PSS channels. The key difference between the vOECT and the planar organic electrochemical transistors (pOECTs) lies in the definition of the channel length. Previously, the pOECT channel length was defined by the distance between source and drain gold contacts formed in the same plane. This 2D arrangement of transistor contacts limits the number of transistors, which may be fabricated in a given area, i.e., device density. Additionally, the channel length is limited by the fabrication process, typically to around $5 \mu\text{m}$. The vOECT channel length, L , is defined by the thickness of the parylene-C (PaC) dielectric layer separating the vertically stacked source and drain contacts, allowing for sub-micrometer resolution (here L was varied down to 450 nm). This is illustrated in **Figure 1**. As seen in **Figure 1b**, the exposed gold contact width defines the channel width, W , while the intermediate PaC layer thickness defines L .

Fabricated vOECTs exhibit very high transconductance as well as good cutoff frequency. This was characterized through steady-state (direct current, DC) and transient (alternating current, AC) measurements, performed on all vOECT and pOECT device variations. Steady-state characterization was performed by measuring the output (sweeping the drain–source bias, V_D , from 0 to -0.6 V and stepping the gate–source bias, V_G , from -0.2 to 0.6 V) and transfer (sweeping V_G from -0.2 to 0.6 with $V_D = -0.6 \text{ V}$) characteristics. The transfer characteristics were subsequently utilized to extract the transconductance of various OECT channel geometries. As demonstrated by Rivnay et al., OECTs store charge in the bulk of PEDOT:PSS rather than at an interface, and their transconductance depends on Wd/L , where d is the thickness of the PEDOT:PSS film and W and L are the channel dimensions.^[11] The inversely proportional relationship between transconductance g_m and channel length L holds true for other transistor technologies and has been

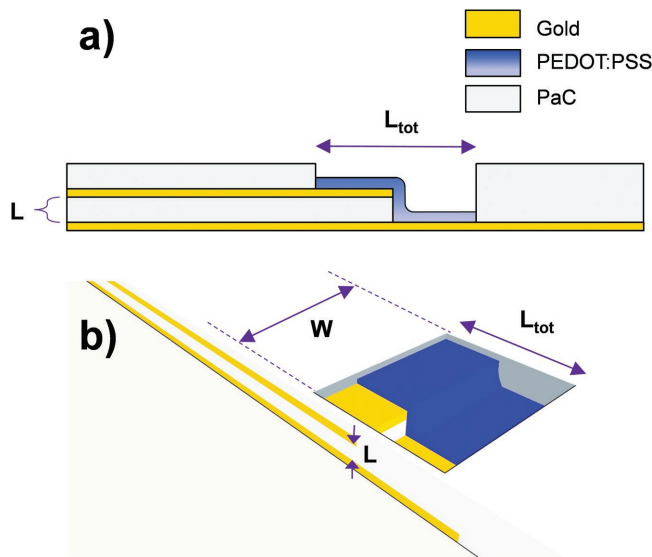


Figure 1. vOECT structure. a) Cross-sectional view demonstrating how the PaC layer thickness defines the channel length (L). b) Top view with PEDOT:PSS shown partially filled in, to aid in the visualization of L . W and L_{tot} are defined by the PaC opening, L_{tot} is specified for calculation of the total PEDOT:PSS layer volume.

extensively studied in both inorganic^[33] and organic field-effect transistors (FETs),^[3] where the thickness of the semiconductor layer, d , does not play a role. This inverse proportionality with L led to the concept of the vertical transistor where L can be substantially reduced, benefiting from increased inherent transistor amplification. To demonstrate these benefits, pOECTs and vOECTs were fabricated with the same channel widths ($W = 70 \mu\text{m}$) to allow for direct comparison. **Figure 2a** illustrates the dramatic increase in g_m for the vOECT (up to 24 mS for $L = 450 \text{ nm}$) while using less than half of the substrate area necessary for the pOECT. **Figure 2b–e** shows SEM images of the pOECT and vOECT and corresponding schematics illustrating the W and L of the transistors.

The vOECT transfer characteristics were measured for various channel lengths ($L = 450 \text{ nm}–1.4 \mu\text{m}$) and two PEDOT:PSS thicknesses ($d = 70 \text{ nm}, 180 \text{ nm}$). The transconductance was obtained by taking the derivative of the transfer characteristic.

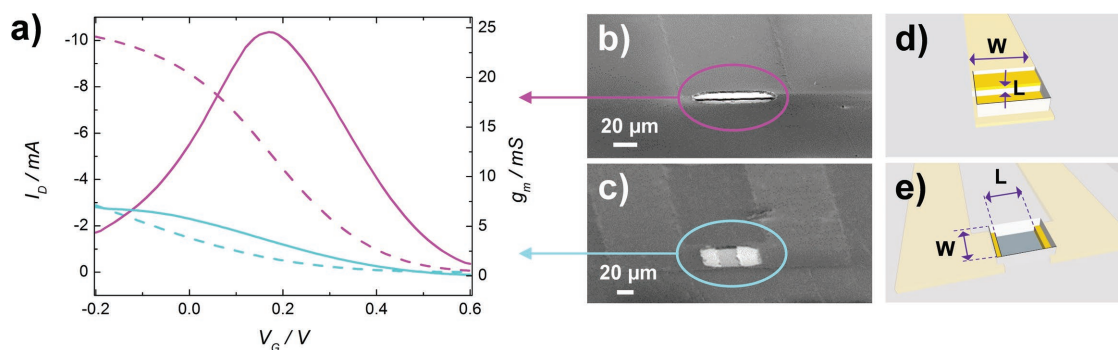


Figure 2. vOECT versus pOECT. a) Demonstration of increased vOECT amplification through transfer characteristics (dashed lines) measured at $V_D = -0.6$ and their derivatives (transconductance, g_m , solid lines). Magenta and cyan lines correspond to the vOECT and pOECT, respectively. The vOECT in (b) and (d) utilizes less substrate space than the pOECT in (c) and (e) as seen by SEM and sketched in 3D.

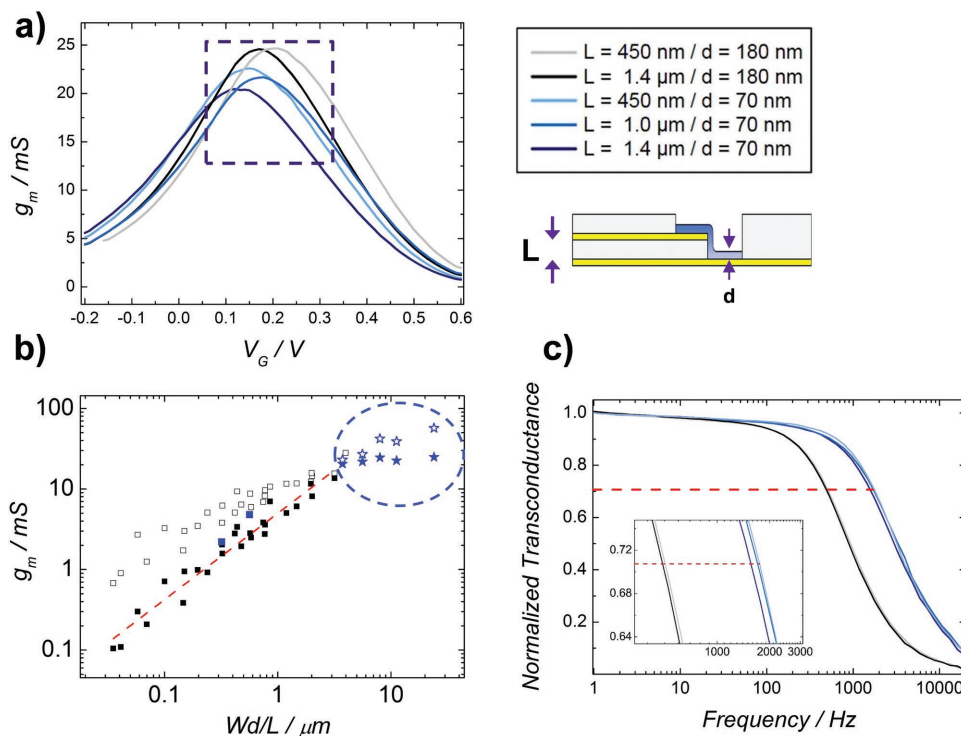


Figure 3. Scaling of transistor transconductance with channel length (L) (i.e., PaC thickness). a) The increase in peak transconductance (g_m) and corresponding legend. b) Peak vOECT g_m values are overlaid on previous pOECT data.^[11] Blue stars represent vOECT devices, with filled and empty symbols indicating measured (g_m) and intrinsic (g_{mi}) transconductance, respectively. Blue squares represent pOECT data obtained in this study. c) Frequency response of vOECTs with the zoomed-in cut-off frequency in the inset.

The scaling of g_m with decreasing L (PaC thickness) is shown in **Figure 3a,b**. To correlate vOECT and pOECT geometries, the peak transconductance values for each Wd/L are shown in **Figure 3b**. Here, the vOECT peak g_m values (star symbols) are overlaid with past pOECT data.^[11] The vOECT geometry leads to higher values of Wd/L , previously unattainable with the pOECT layout and standard lithography. However, slight deviation from the fit is also observed. This effect becomes particularly evident as the channel length is shortened and/or the PEDOT:PSS thickness is increased, thus leading to higher values of Wd/L . This deviation results from the parasitic series resistance which in our case is mainly due to the contact lines, namely, the source–drain series resistance, R_{SD} . This effect and the resulting difference between measured (g_m) and intrinsic (g_{mi}) transconductance has been investigated previously for short channel FETs.^[34] For instances of nonzero drain conductance (due to short-channel effects or the transistor not being in saturation mode) the intrinsic transconductance, g_{mi} , was found to be

$$g_{mi} = g_m^0 / (1 - R_{SD}g_d(1 + R_s g_m^0)) \quad (1)$$

where g_d is the drain conductance ($g_d = \partial I_D / \partial V_D$), and g_m^0 is

$$g_m^0 = g_m / (1 - R_s g_m) \quad (2)$$

with g_m representing the measured transconductance ($g_m = \partial I_D / \partial V_G$). Equation (2) is accurate only when $g_d = 0$, and it may be seen that Equation (1) reduces to Equation (2) when this is the case. Contact line resistances of the vOECT devices used in this

study were both calculated and measured. The drain conductance was found from the OECT output characteristics for $V_D = -0.6$ V. The drain conductance and source/drain series resistance were utilized to calculate the intrinsic transconductance of vOECTs according to Equation (1) (Figure S1, Supporting Information). The obtained peak g_{mi} values are represented by open star symbols in **Figure 3b**. These intrinsic transconductance values follow the previous trend, while reaching values of Wd/L previously unseen in OECTs. Although a potential additional issue could result from the contact resistance of the devices (i.e., the PEDOT:PSS/Au contact), the scaling of g_m as expected with reduced device dimensions indicates negligible effects due to this interface. Intrinsic transconductance values of up to 57 mS were found, which translates to 814 S m^{-1} when normalized to the channel width (g_m/W), the highest reported value for OECTs to date.^[32] This geometry-normalization represents a method to compare transistor amplification properties while considering the device footprint.

Good transient response of vOECTs is shown through the normalized transconductance as a function of AC frequency, compared for different transistor geometries. In a past study the cut-off frequency (f_T) of pOECTs was determined to depend on the PEDOT:PSS layer volume,^[11] namely

$$\frac{1}{2\pi f_T} \sim d \cdot (WL_{tot})^{1/2} \quad (3)$$

where d is the PEDOT:PSS thickness and W and L_{tot} are the PEDOT:PSS channel dimensions. This means that the entire

PEDOT:PSS film (thickness, as well as planar dimensions—i.e., the surface area in contact with the electrolyte) affects the device performance. Typically, the overlap of PEDOT:PSS on the gold electrodes of pOECTs has been negligible in comparison to the channel length and L_{tot} may be approximated by L . Consequently, reduction in the PEDOT:PSS thickness and/or transistor dimensions (L and W) leads to an increased cut-off frequency. In the case of vOECTs, the polymer/gold electrode overlap must be taken into account and the entire PEDOT:PSS volume is calculated using L_{tot} as indicated in Figure 1b. Our vOECTs exhibited cut-off frequencies between 1.3 and 1.7 kHz for $d = 70$ nm and ≈ 550 Hz for $d = 180$ nm (Figure 3d). These results fall short of the values obtained utilizing Equation (3) by a factor of 3 to 4 (f_T values estimated from previous data and Equation (3) are ≈ 5.5 and 2.3 kHz for the 70 and 180 nm PEDOT:PSS films, respectively).^[11] This is likely due to additional parasitic resistance/capacitance as a result of interconnects and polymer/electrode overlap. However, source/drain series resistance and some amount of overlap (i.e., additional capacitive effects) are ultimately unavoidable, particularly in situations of limited substrate space. Thus, vOECT transient device performance indicates that higher cutoff frequencies may be obtained as the channel dimensions are reduced (thereby reducing the total volume), while conserving high amplification. These enhancements of the OECT are ideal for implantable devices.

A 3D fabrication process for OECTs has been demonstrated which, when seen from a top down perspective, consolidates all three terminals of a transistor (source/drain and local gate if desired) into a single line perpendicular to the substrate. This dramatically decreases the spatial footprint required by each transistor and provides a pathway for transistor miniaturization. Additionally, the reduced channel length improves transconductance compared to planar OECTs. We have demonstrated vertical OECTs with geometry-normalized intrinsic transconductance greater than 800 S m^{-1} and with cut-off frequencies exceeding 1.5 kHz. These values represent a significant improvement over planar OECTs and can be further enhanced by reducing parasitic effects such as the overlap between the electrolyte and the source/drain contacts. Ultimately, we have shown a path toward high-density, high-performance OECT arrays that will enable spatially and temporally resolved neural interfacing and high-throughput biological assays.

Experimental Section

vOECT/pOECT Fabrication: The fabrication process is based on methods reported previously.^[32] Metal interconnects were photolithographically patterned on glass microscope slides using a positive photoresist (Shipley 1813), a SUSS MJB4 UV broadband contact aligner and MF26 developer (refer to the fabrication schematic in Figure S3, Supporting Information). A 2 nm chromium adhesion promoting layer and 100 nm of gold were thermally evaporated onto the substrates and interconnects were then defined through lift-off. A parylene-C (PaC) film was deposited on the glass slides to thicknesses of 450 nm–1.4 μm (defining the channel length, L) using an SCS Labcoater 2 with 3-(Trimethoxysilyl)propylmethacrylate present in the chamber to act as an adhesion promoter. For the vOECTs a second set of interconnects were patterned on top of the first PaC layer, defined analogously to the first metal lines and overlapping these to create the vertically stacked source and drain contacts. Insulating and sacrificial PaC layers were subsequently

deposited, both to thicknesses of 2 μm . Prior to the sacrificial PaC layer, a dilute solution of Micro-90 industrial cleaner was spin-coated onto the insulating PaC. This allowed the sacrificial layer to later be peeled from the substrate, defining the OECT channel. The PaC layers were etched by reactive ion etching in an Oxford 80 Plasmalab plus with an O_2/CHF_3 plasma to open contact pads and to create an opening down to the source/drain electrodes. These are overlapped in the case of the vOECT and this etching step simultaneously exposes the source/drain electrodes, while establishing the channel length, L . The exposed width of the gold contacts defines the channel width, W . AZ9260 photoresist was utilized as an etch mask, using the UV contact aligner and AZ developer. A dispersion of PEDOT:PSS (Clevios PH 1000 from Heraeus Holding GmbH), 5 vol% ethylene glycol, 0.1 vol% dodecyl benzene sulfonic acid, and 1 wt% of (3-glycidyloxypropyl)-trimethoxysilane was spin-coated onto the substrates to attain a thickness of 70 or 180 nm, coating the vOECT vertical source/drain step or the planar channel area of the pOECT. The sacrificial PaC layer was peeled off removing superfluous PEDOT:PSS and defining the OECT channels. The devices were baked for 1 h at 140 C to crosslink the film. Finally, the devices were immersed in deionized water to remove low molecular weight compounds.

vOECT/pOECT Characterization: All OECT electrical characterization was carried out in 0.1 M NaCl aqueous solution with an Ag/AgCl pellet (Warner Instruments) gate electrode. A National Instruments PXIe-1062Q system with a PXIe-4145 source measure unit was used along with custom LabVIEW software to carry out steady-state and transient measurements. This provided OECT output (sweeping the drain-source bias, V_D , from 0 to -0.6 V and stepping the gate-source bias, V_G , from -0.2 to 0.6 V) and transfer (sweeping V_G from -0.2 to 0.6 with $V_D = -0.6$ V) characteristics. A Keithley 2612A dual SourceMeter was utilized for the measurement of drain conductance used in the intrinsic transconductance calculation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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