College of Engineering & Applied Science
UNIVERSITY OF COLORADO **BOULDER**

Node Network Time Synchronization

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Objective

High precision time synchronization within a complex suite of subsystems is crucial for the operation of an aircraft's Onboard Communication System (OCS). The Node Network Time Synchronization (NNTS) System seeks to accomplish this by using the IEEE 1588 PTP algorithm to calculate the time delay between multiple nodes with respect to one Node (the Master) and adjust the phase of each of their clocks, effectively achieving synchronization.

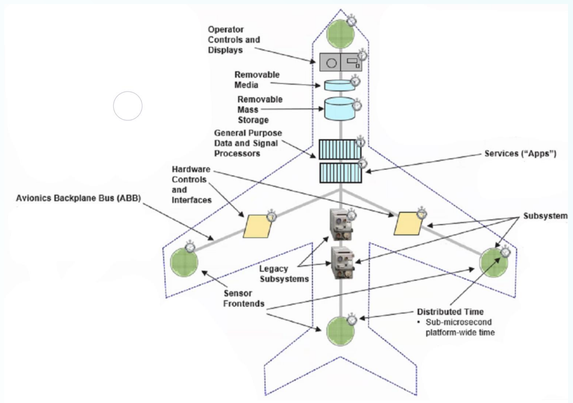
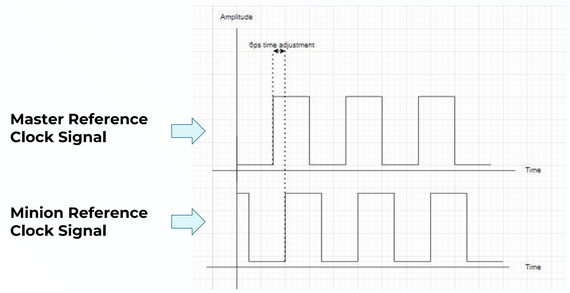


Figure 1. Onboard Communication System (OCS) Subsystems

Phase Adjustment

The key to successful time synchronization relies on continuously adjusting the clock cycles of all subsystems comprising the OCS. Synchronizing multiple clocks is accomplished through phase adjustment operations. One of the subsystems within the OCS is designated the "Master Node" and all other subsystems are "Minion Nodes." The phases of all Minion clocks are adjusted using the Master Node as a reference.



What Our Project Is

Clock Adjustment System

- We designed a Clock Synchronization System that will adjust a node's clock to sub nanosecond precision.
- Our system can take in certain adjustment data (i.e. differential in timestamps) and then will calculate and adjust the clock by the corresponding phase.
- Our system's clock adjustment is done at the hardware level in order to obtain optimal precision
- Our system is developed to be directly integrated into an Ethernet Network that is utilizing IEEE 1588 PTP.
  - The only thing that is needed is an Ethernet UDP Driver with abstracted send and receive functions that handle 1588 Event Frames
    - The abstracted functions should take in the 1588 Event Frame message type as an argument
    - With these functions, a differential can be calculated with the 1588 algorithm and then used in our system to perform time synchronization
  - Our system will work with any Ethernet Network that has 1588 PTP implemented and will perform the clock adjustment to obtain synchronization

How It Works

Overview:

- Master and Minion Nodes are connected via ethernet.
- Minion Node's microcontroller receives adjustment data from the Master Node.
- Microcontroller uses that data and performers calculations to send the correct adjustment signals to the CSU (Clock Synchronization Unit)
- Reference clock and adjustment signals (Delay Control and Lead Lag) are fed into the CSU.
- CSU adjusts the phase of the clock to line up rising edges with the reference clock to 1/768th of a Unit Period precision.
- CSU outputs adjusted clock waveform to be fed into its respective subsystem.

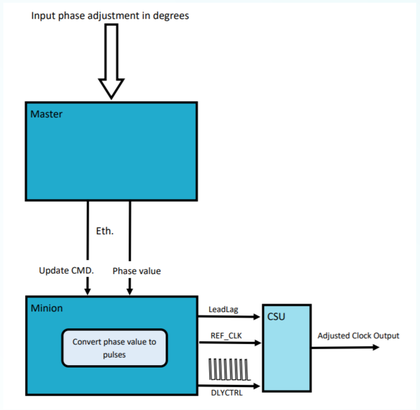
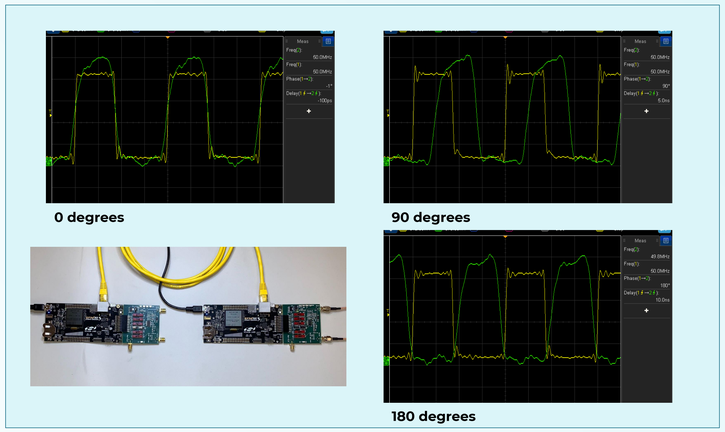


Figure 2. NNTS Functional Diagram



0 degrees **90 degrees** **180 degrees**

Figure 3. Oscilloscope display, showing phase shift at 0, 90, and 180 degrees

Note: Clock buffers on the output signal (yellow) creates a clean square wave

Printed Circuit Board

- Phase shifting system utilizing a **Phase Locked Loop (PLL)**
  - Reference Clock
  - DLYCTRL - Rising edges shift phase by a fraction of a time period (Calculated in software).
  - LEADLAG - Shifts the signal forward or backward.
- Maintains signal integrity and reduces noise using a clock buffer and second order filters.

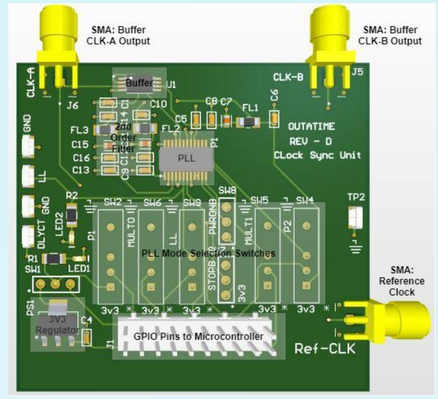


Figure 4. Clock Synchronization Unit (CSU)

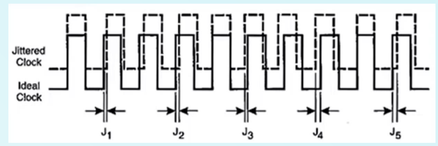


Figure 5. TI CDCF5801A has an **8 ps phase jitter @500 MHz**

Software

- Take in timestamps from Master Node and calculate the proper adjustments needed to phase align the clock signal.
- Abstracted functions were written to create the correct control signals for any adjustment amount

Degrees	Rising Edges	Edges Missed	Degrees Missed
1	2.1	0.1	0.0
5	10.7	0.3	0.2
10	21.3	0.7	0.3
45	96.0	3.0	1.4
90	192.0	6.0	2.8
180	384.0	12.0	5.6

Table 1. Delay Control Signal Error according to the PLL data sheet