CANVAS CDR
Summer 2020 Review

Agenda

CANVAS Presentation Schedule			
Section	**Presenter**	**Time**	**Duration**
Introduction	Kyle	12:30 PM	0:05
S/C Overview and Mission Design	Kyle	12:35 PM	0:25
Instrumentation Intro	Riley	1:00 PM	0:05
E-Field Antennas	Kyle / Riley	1:05 PM	0:10
E-Field Pre-Amps	Keith	1:15 PM	0:05
B-Field Search Coils and Holder	Kyle / Riley	1:20 PM	0:05
B-Field Pre-Amps	Riley	1:25 PM	0:10
Analog Receiver Board	Riley / Keith	1:35 PM	0:15
Digital Receiver Board	Sebastian	1:50 PM	0:15
FPGA Development	Sebastian	2:05 PM	0:10
10 Minute Break, return at 2:25pm			
Structures			
Bus Overview	Dhruv	2:25 PM	0:05
Fasteners and Analyses	Dhruv	2:30 PM	0:10
CTD Boom	Kyle	2:40 PM	0:05
Thermal	Shab	2:45 PM	0:10
Subsystems Part 1			
Power Budget, Solar Panels, Batteries	Ryan	2:55 PM	0:10
EPS	Jett	3:05 PM	0:10
CDH	Chadd	3:15 PM	0:15
GSE	Max	3:30 PM	0:10
COMMs	Kyle	3:40 PM	0:05
S-Band / GPS Daughter Board	Jett	3:45 PM	0:05
Back Plane and Wiring	Dhruv / Jett	3:50 PM	0:10
5 Minute Break, return at 4:00pm			
Subsystems Part 2			
ADCS / XACT	Kyle	4:05 PM	0:05
FSW	Lea	4:10 PM	0:05
Systems and Management			
Integration and Testing	Kyle	4:25 PM	0:05
Risk Analysis	Kyle	4:30 PM	0:10
Budget and Schedule	Kyle	4:40 PM	0:10
Questions and Feedback		4:50 PM	0:10
	End / Total	**5:00 PM**	**4:30**

Team Organization

Advisor/Customer:
Dr. Robert Marshall

Advisor:
Dr. Nick Rainville

Project Manager:
Kyle Nieukirk

Instr. Lead:
Riley Reid

Instr.:
Keith Poletti

Electrical Eng.:
Sebastian Wankmueller

FSW Lead:
Lea Chandler

Structural Lead:
Dhruv Chawla

Thermal Lead:
Shab Rajasekaran

ADCS Lead:
Kyle Nieukirk

CDH Lead:
Chadd Miller

EPS Board Lead:
Jett Moore

Solar Panel Lead:
Ryan Burdick

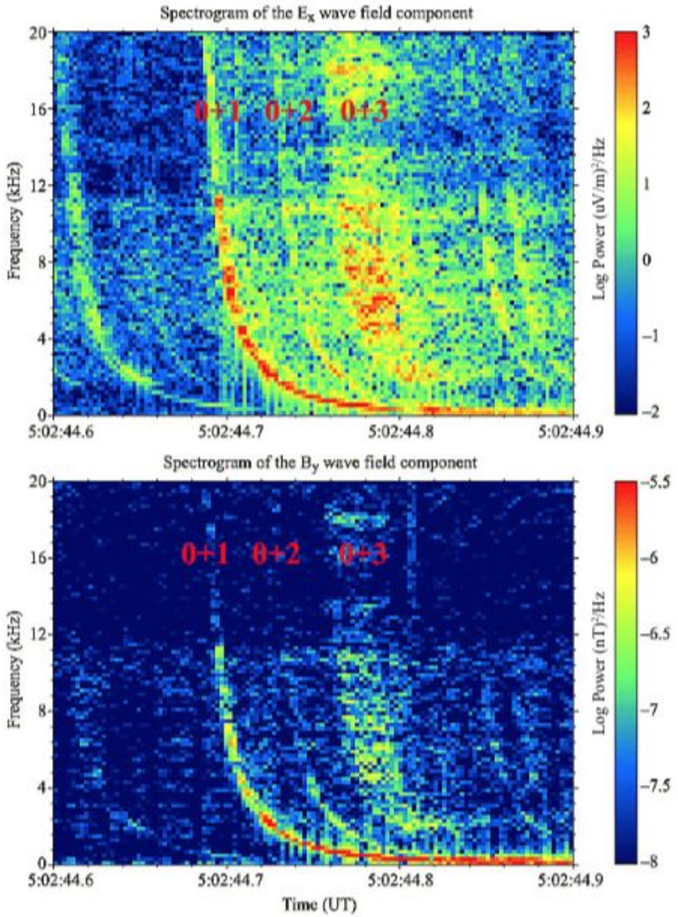
GSE Lead:
Max Fidler

Science Background

SQ1) What is the electromagnetic energy input into the space environment by **lightning and ground-based VLF transmitters?**

SQ2) What is the frequency spectrum of VLF wave energy above the ionosphere in the **0.3–40 kHz range?**

SQ3) What is the **transmission transfer function** of the ionosphere for VLF energy, and how does it vary in space and time?



Example whistlers from DEMETER; Lefeuvre et. al [2009]

Science Requirements

SQ1) EM Energy Input → VLF Wave Power and k-direction

SQ2) Frequency Spectrum → VLF Wave Spectra

SQ3) Transfer Function → VLF Wave Spectra and Amplitude

→ Additional data processing - SVD methods

- Frequency range: 0.3-40 kHz
- Uniform gain within 3 dB

- Min. E-field sensitivity 10^{-6} V/m/Hz$^{1/2}$
- Min. B-field sensitivity 10^{-4} nT/Hz$^{1/2}$
- Min. E- & B-field SFDR 50 dB > sensitivity requirement

- Wave component directions known within 1 degree
- Position knowledge better than 10 km

Mission Design and Spacecraft Overview

Kyle

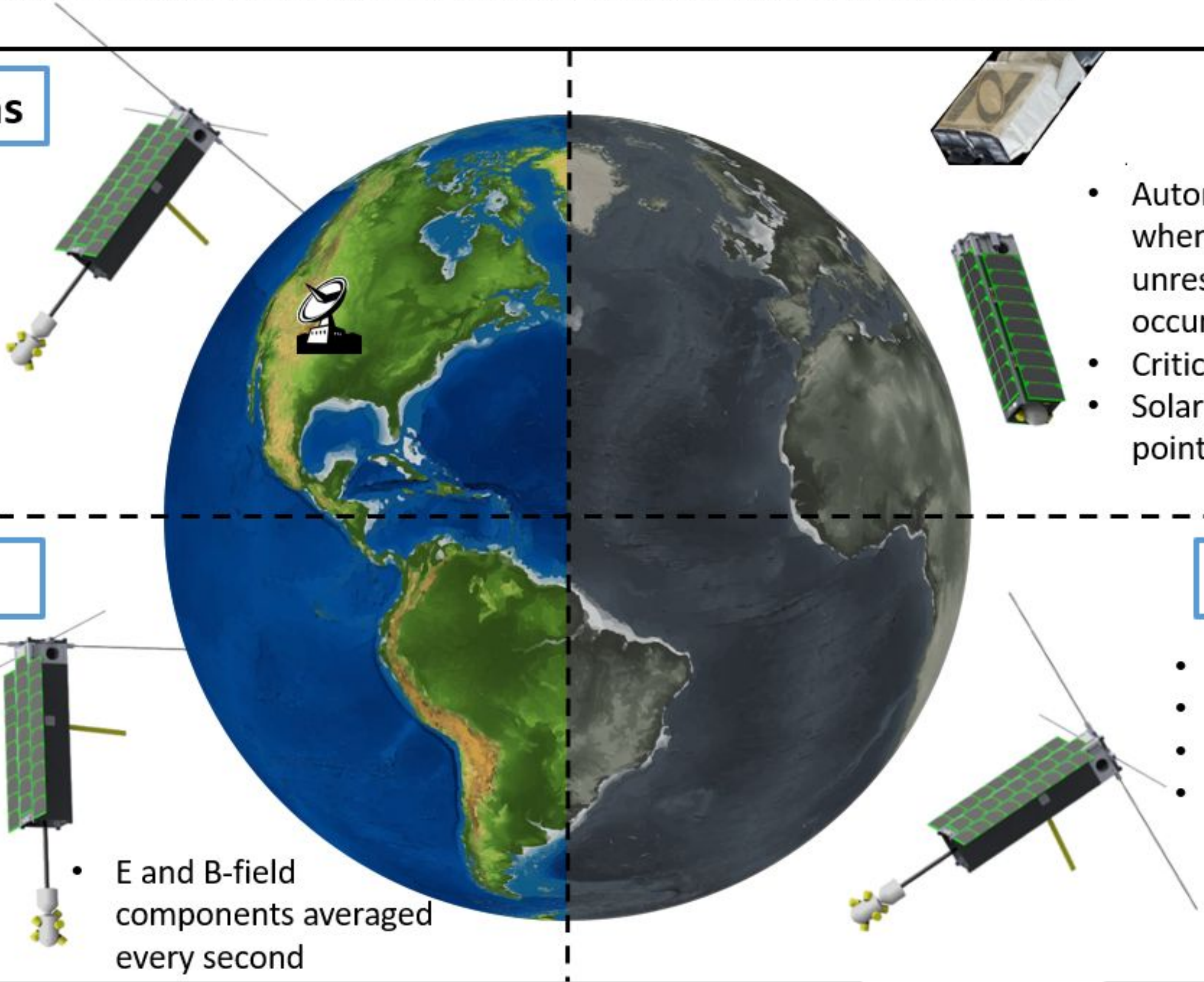
Mission Design

Mission Element		
	Acceptable	**Designing For**
Altitude	450-550 km	500 km
Inclination	50-55°	51.6°
Duration	1 year	
Comm	UHF and S-Band	
Ground station	LASP	

Additional Req's:

- CANVAS shall be limited to a total orbit lifetime of less than 25 years.
- CANVAS shall not operate any system for a minimum of 30 minutes where hazard potential exists.
- CANVAS deployables will be deployed after the 30 minute time period once the spacecraft has de-tumbled (0.5 deg/sec) and been switched into Normal Operations Mode.

All Modes: CDH, EPS, GPS, ADCS, UHF Rx, and TCS always on. Telemetry beacon every 16s.



Communications

- UHF and S-band on, pointing towards LASP
- S-band data downlink
- UHF command uplink

Safe Mode

- Automatically entered when SOC <60% or unresolvable error occurs
- Critical components on
- Solar panels sun pointing

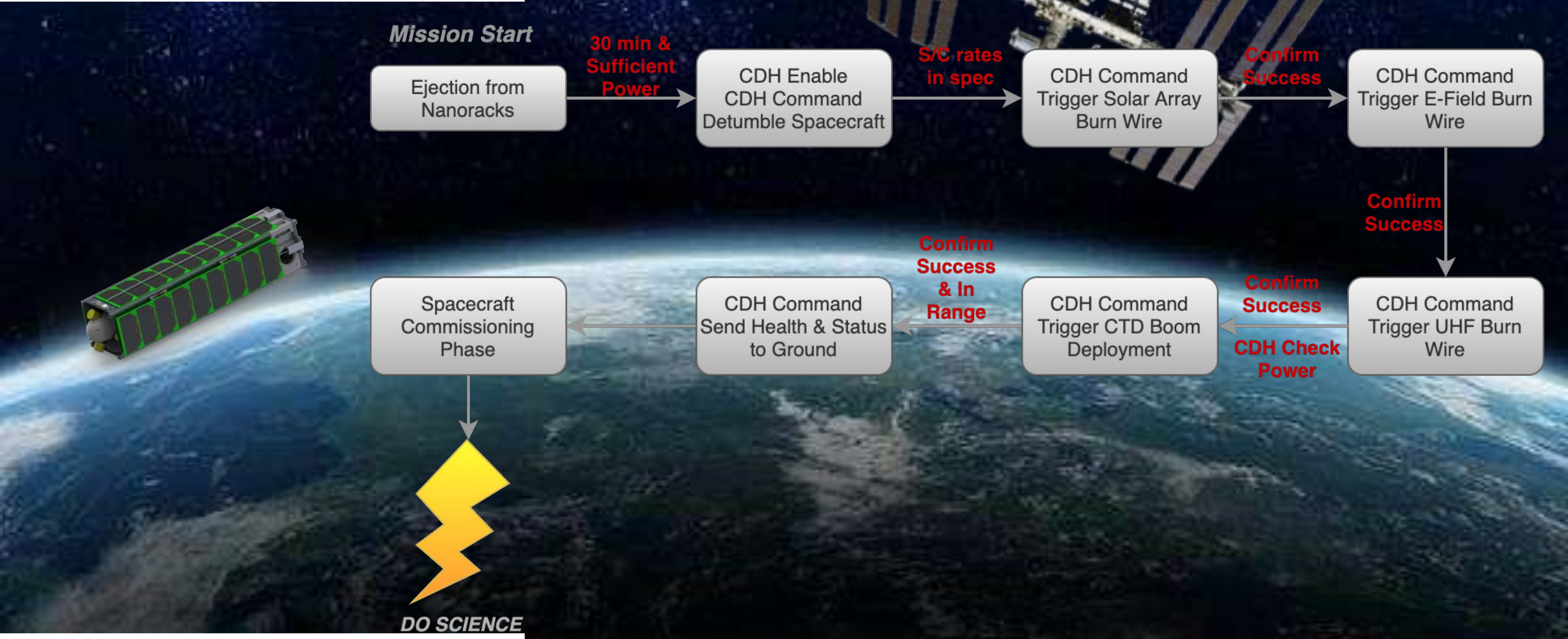
Normal Mode

- Solar panels sun-pointing day side
- Payload WMM tracking night side
- E and B-field components averaged every second

Deployment

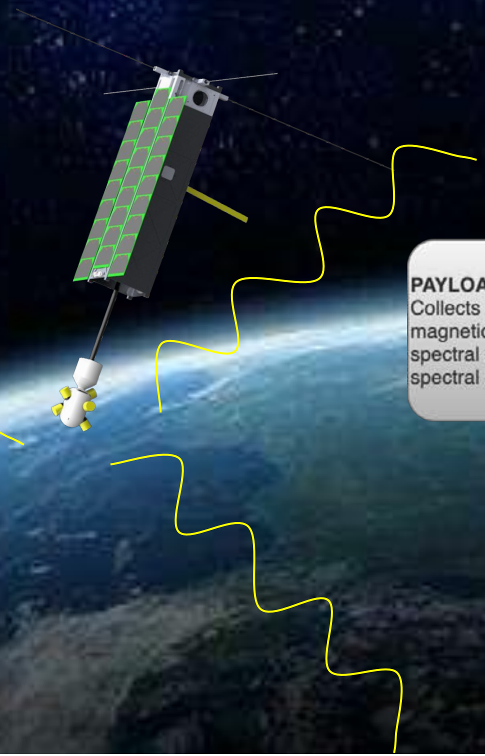
- Solar Panels
- E-Field Antennas
- UHF Antenna
- CTD Boom

Mission Design
Deployment



Mission Design

Normal Mode



PAYLOAD
Collects electric and magnetic field spectral and cross-spectral data at 1 Hz

Sunlit
Duration: 60 minutes
Mode Power: ~12 W

- **C&DH**
  Storing payload data
  Health and status monitoring
- **ADCS**
  Align: -Y with Sun
  Constrain: -X with Nadir
- **EPS**
  Power dist from solar array
  Charge/monitor batteries
- **COMM**
  Power-saving standby
  UHF RX/Beacon active
- **THERM**
  Off

Eclipse
Duration: 36 minutes
Mode Power: ~12 W

- **C&DH**
  Unchanged
- **ADCS**
  Align: -X with WMM
  Constrain: -X with Nadir
- **EPS**
  Power dist. from batteries
  Monitor discharge
- **COMM**
  In power saving stand-by
  UHF RX/Beacon active
- **THERM**
  20% duty cycle battery heaters

Entry Criteria:

This the default mode after deployment.

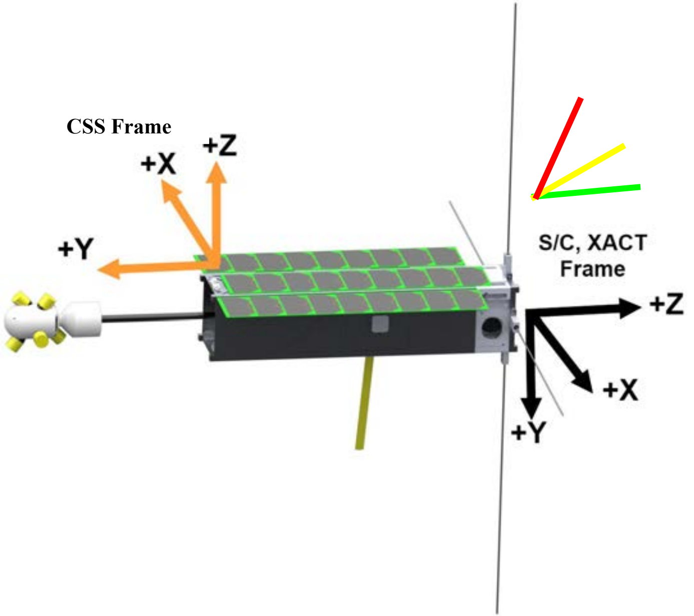
- Spacecraft has deployed successfully
- Spacecraft is not in safe mode
- Spacecraft is not in communication mode
- The spacecraft is not preparing to enter communications mode

Exit Criteria:

- The spacecraft is starting a slew maneuver to prepare for ground communication
- The spacecraft has entered safe mode
- The spacecraft has received a fault that otherwise requires ground intervention

Mission Design Considerations

- Lightning VLF wave are approximately parallel with B-field
  - E-field waves would be perpendicular
  - Ideally, would have E-field Antenna plane perpendicular to the E-field wave propagation
    - Allows for unique solutions of the wave propagation direction
  - Thus want +Z body vector to align with WMM Vector
- “Best” data region is when +Z and WMM are within +/- 30 deg
- “Good” data region is when +Z and WMM are within +/- 3- to 60 deg
- “Bad” data region is above 60 deg off-pointing angle between +Z Body and WMM Vectors

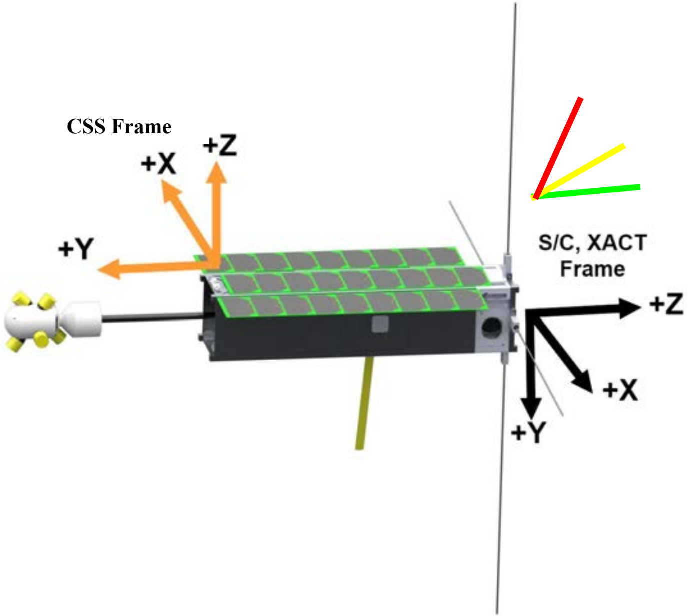


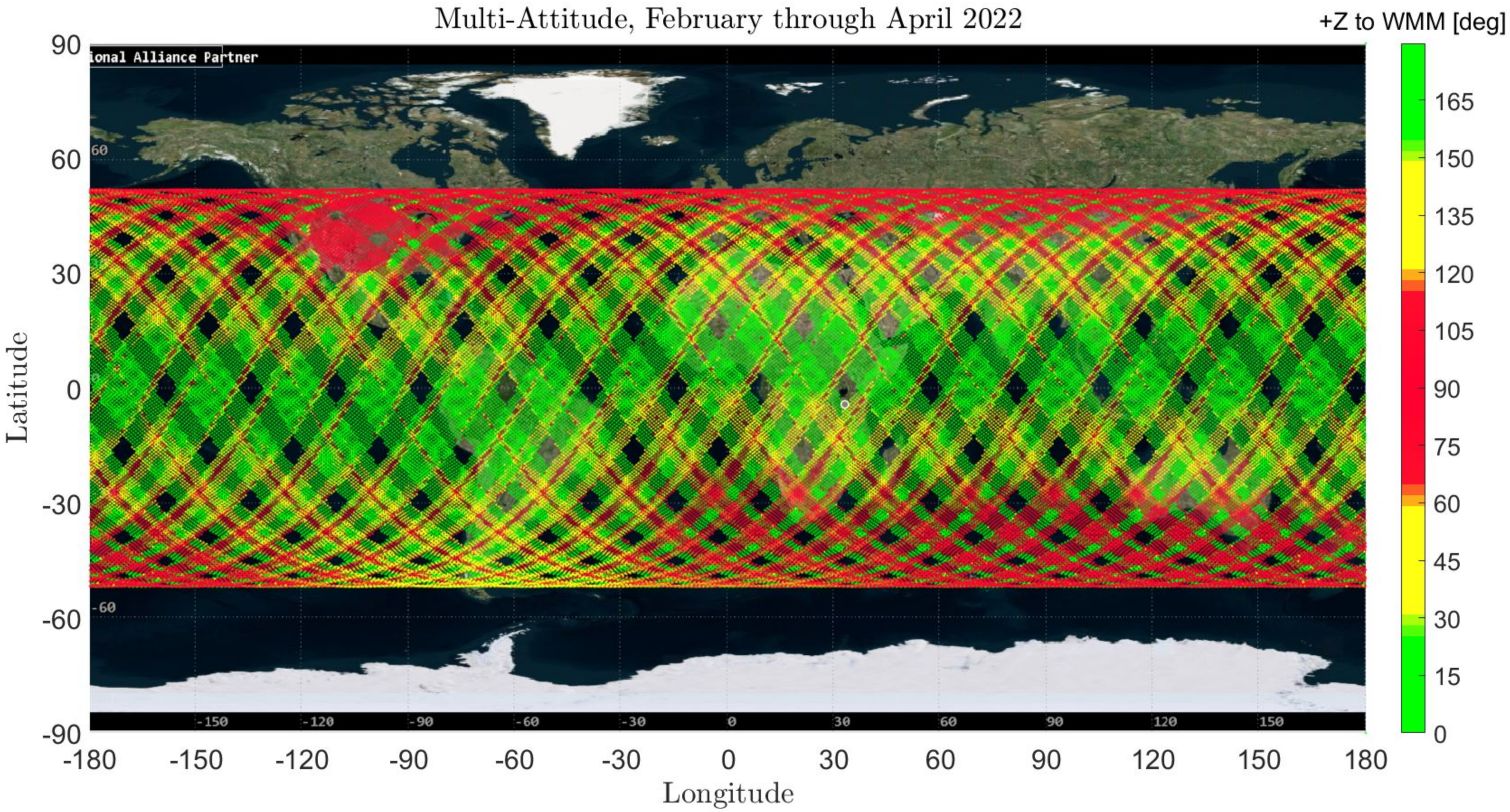
Mission Design Considerations

- In order to meet power requirements, we need -Y Body and Sun Vectors to be aligned during day side
- Must trade off between “good” science data and spacecraft operation

Leads to:

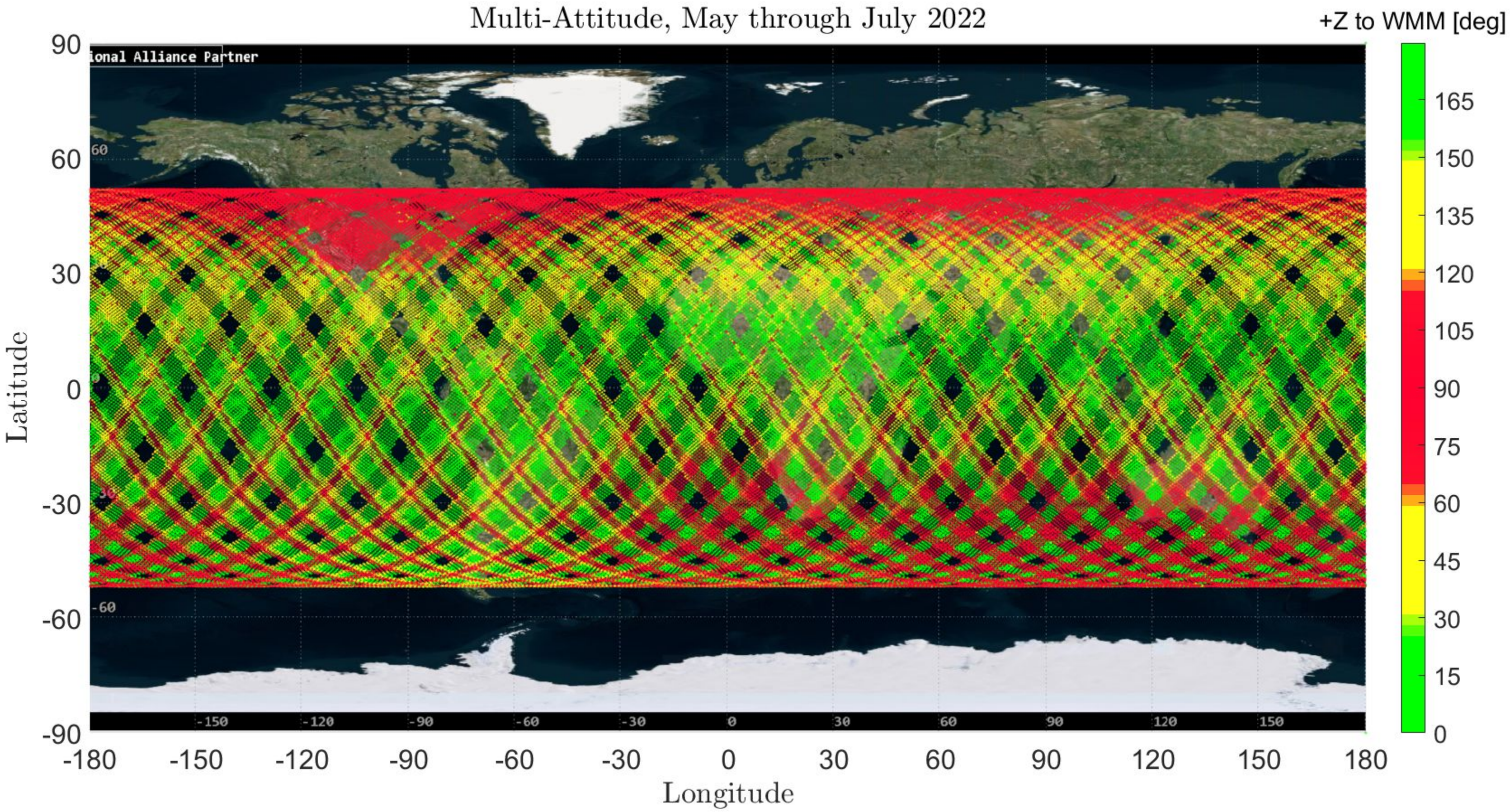
- -Y aligned with Sun during sunlit periods
  - -X constrained to Nadir
- +Z aligned with WMM during eclipse
  - -X constrained to Nadir





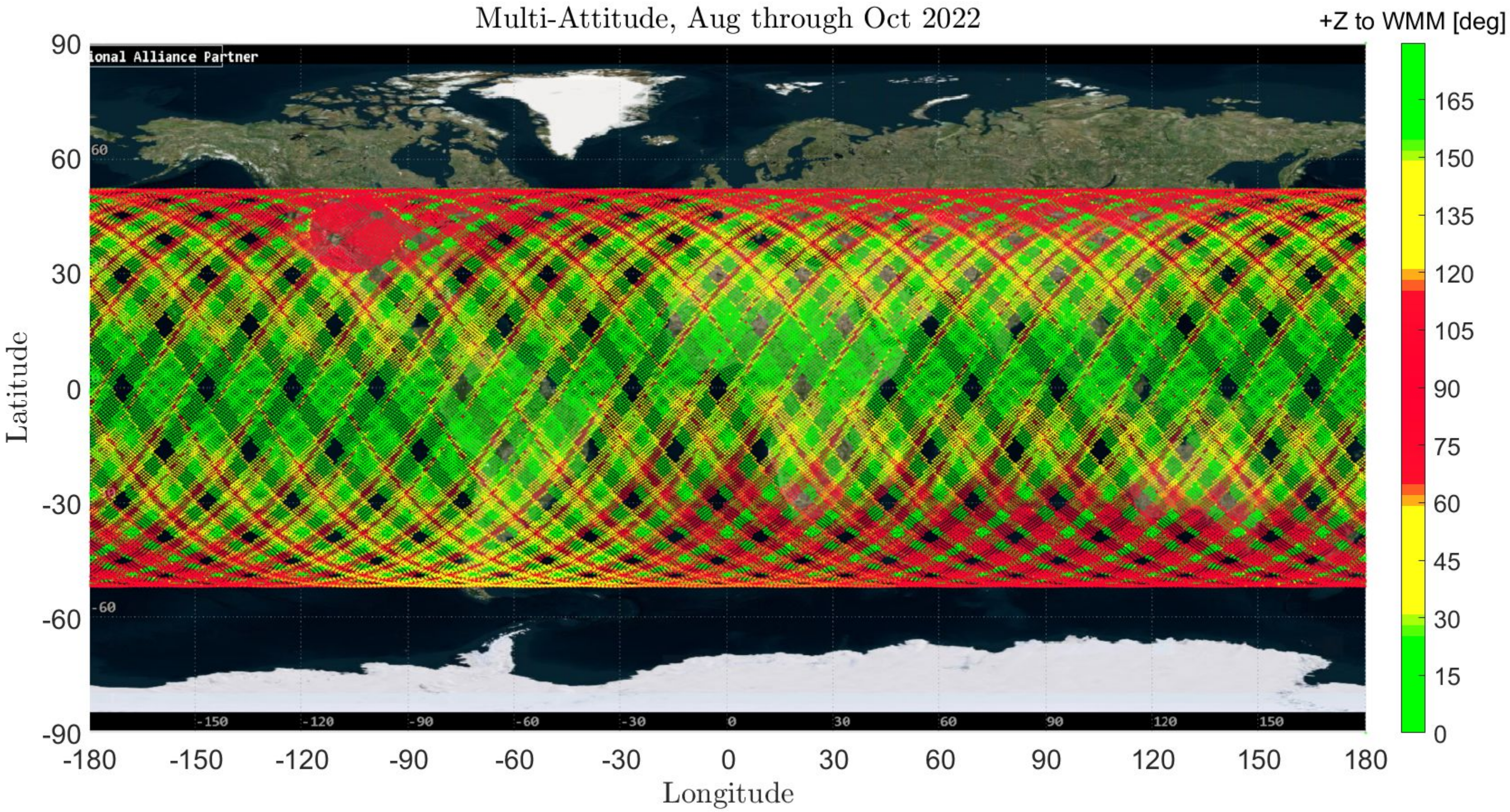
Sun pointing on day side, WMM pointing on night side

Settled on 0-30 deg off parallel as “best,” 30-60 as “good” and 60-90 as “bad”



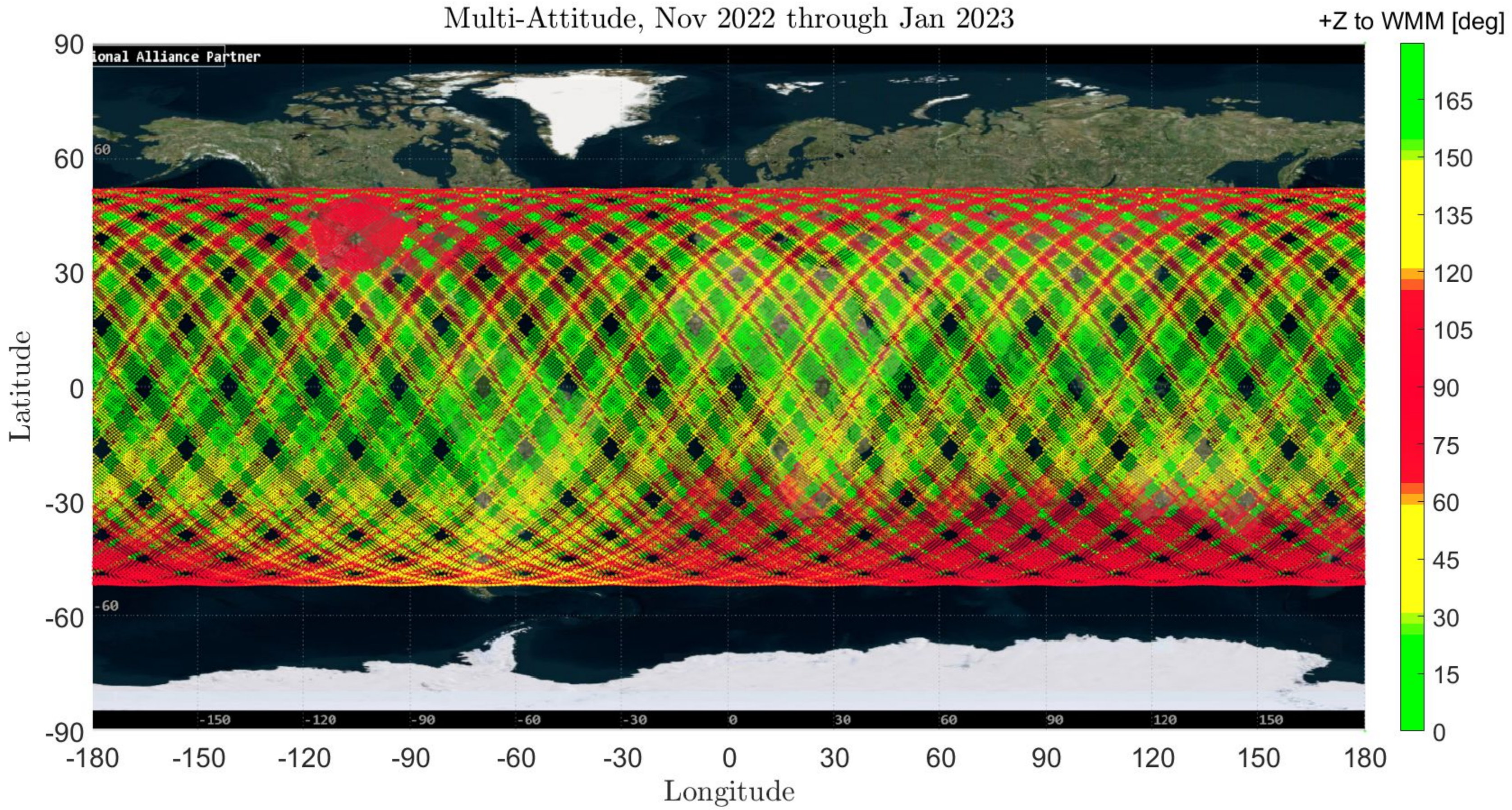
Sun pointing on day side, WMM pointing on night side

Settled on 0-30 deg off parallel as “best,”
30-60 as “good” and 60-90 as “bad”



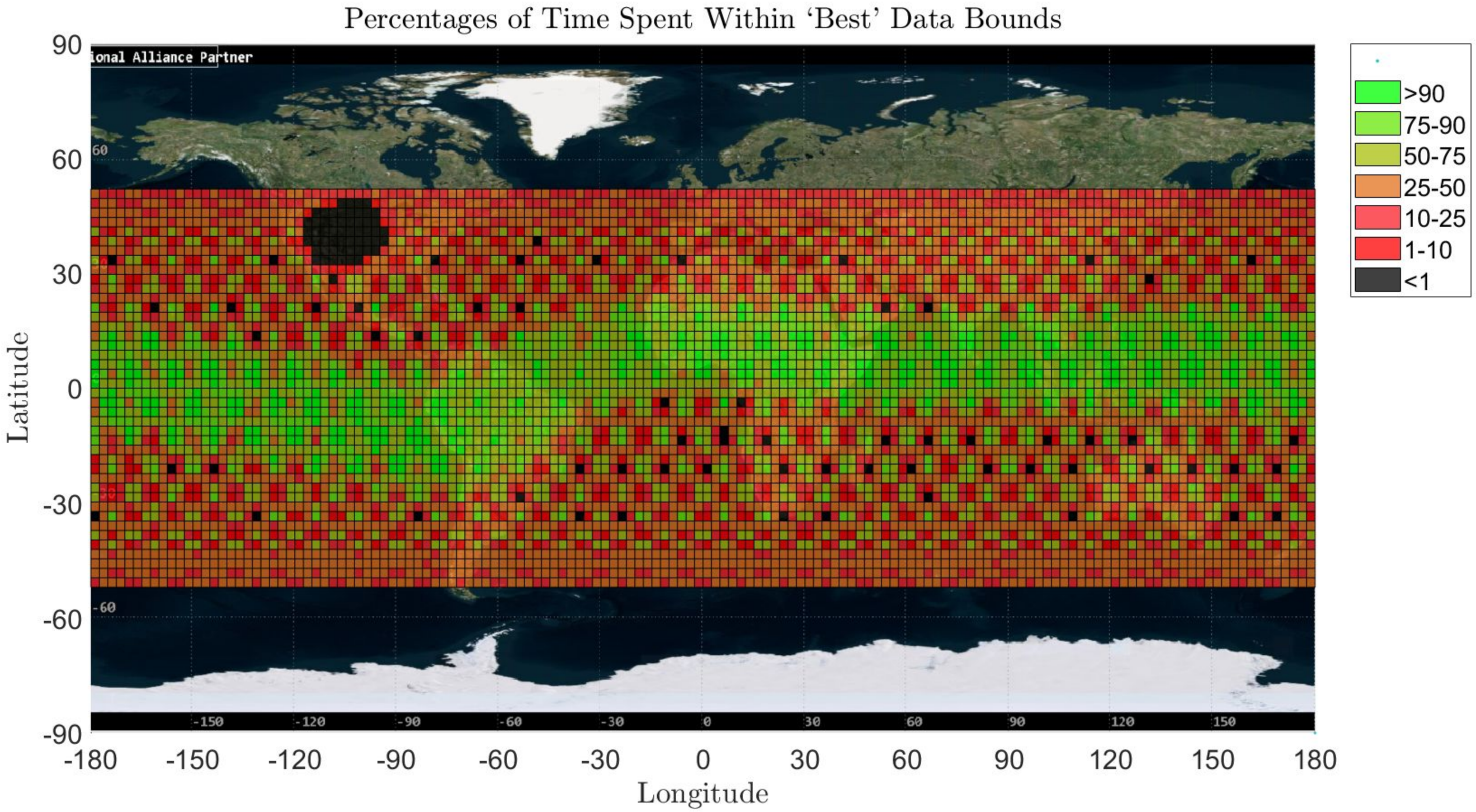
Sun pointing on day side, WMM pointing on night side

Settled on 0-30 deg off parallel as “best,” 30-60 as “good” and 60-90 as “bad”

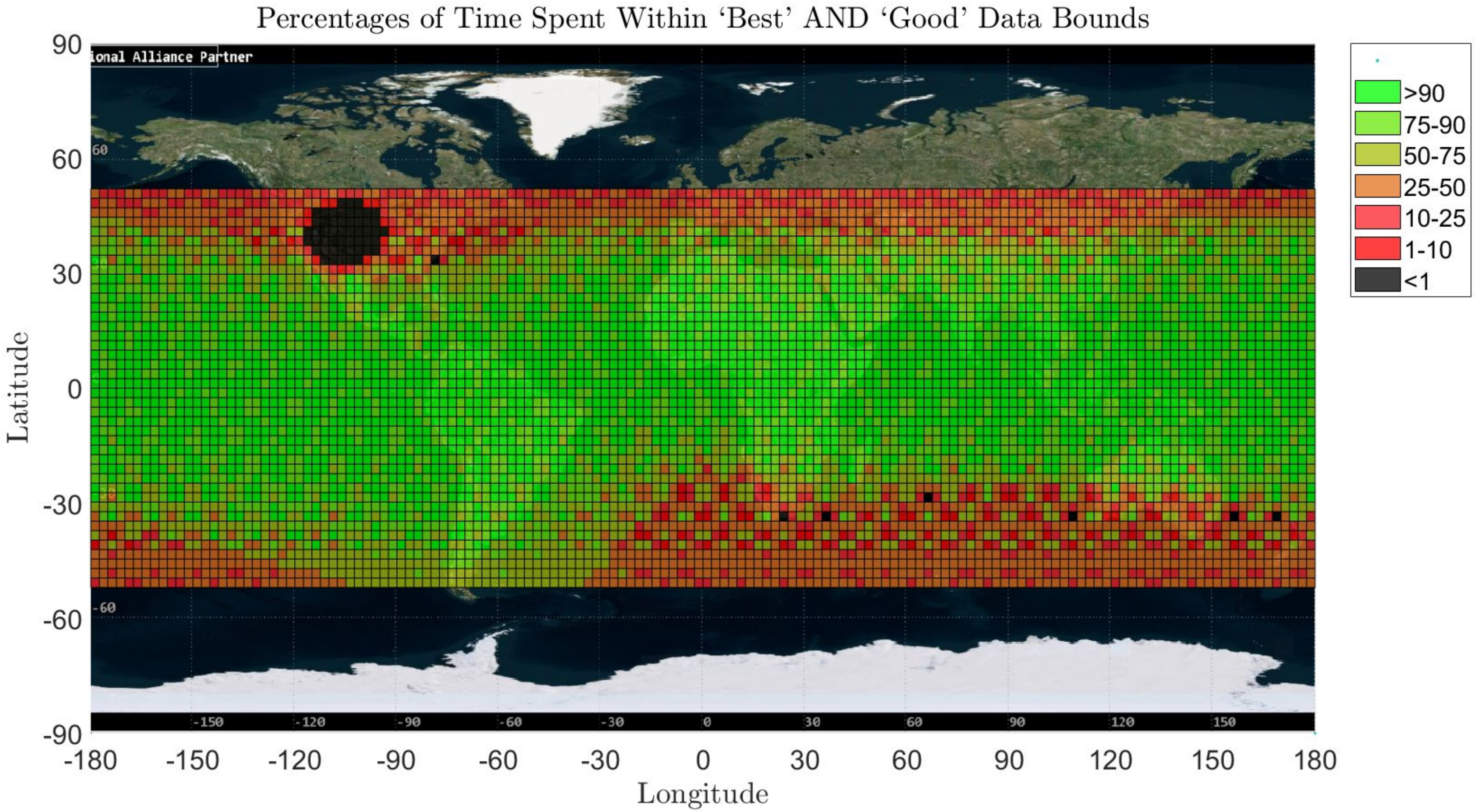


Sun pointing on day side, WMM pointing on night side

Settled on 0-30 deg off parallel as “best,” 30-60 as “good” and 60-90 as “bad”



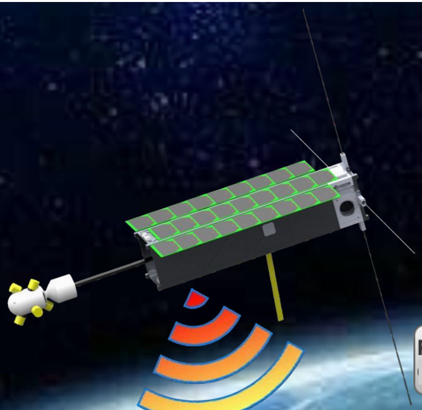
Binned by % of time within the "best" data region



Binned by % of time within the “best” and “good” data regions

Mission Design

Communication Mode



PAYLOAD:
OFF (?)

Sunlit & Eclipse
Duration: 5 minutes
Mode Power: ~14 W

C&DH
Xfer science data from memory to S-Band radio for xmission

ADCS
Ground-station point
Hi-accuracy required

EPS
Power supply and monitoring

COMM
Transmitting received packets from C&DH to ground

THERM
Off

Entry Criteria:

- Spacecraft has deployed successfully
- Spacecraft is not in safe mode
- The spacecraft has reached a scheduled communication maneuver uploaded from the ground station
- The spacecraft is in range of the ground station

Exit Criteria:

- The spacecraft is starting a slew maneuver to prepare for ground communication
- The spacecraft has entered safe mode
- The spacecraft has received a fault that otherwise requires ground intervention

Orbital Radiation

Rad Analysis

- Radiation - Total ionizing dose at 52 degree inclination for 1 year mission
- COTS components durable enough, hardening placed on in-house manufactured electronics
    - At 1mm, 1 year, 6.3 kRad - COTS/Mechanisms/Payload/Comms
    - At 2 mm, 1 year, 1.6 kRad - Electronics Stack

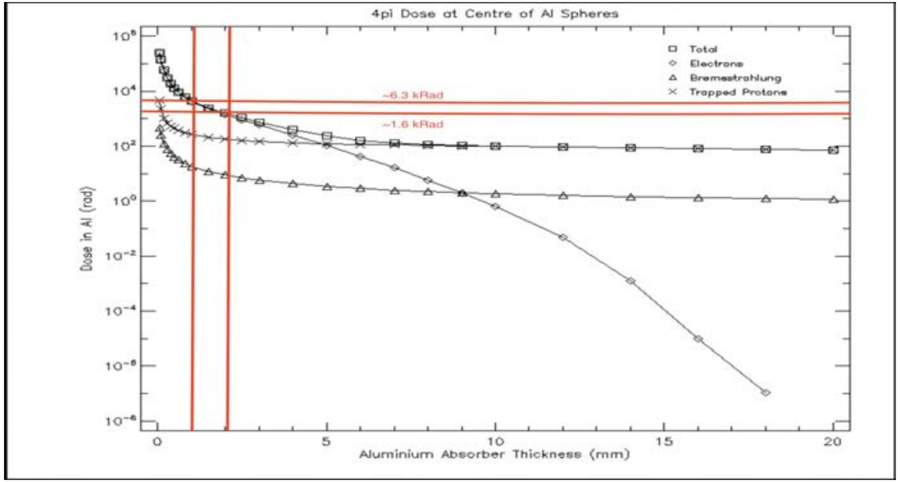
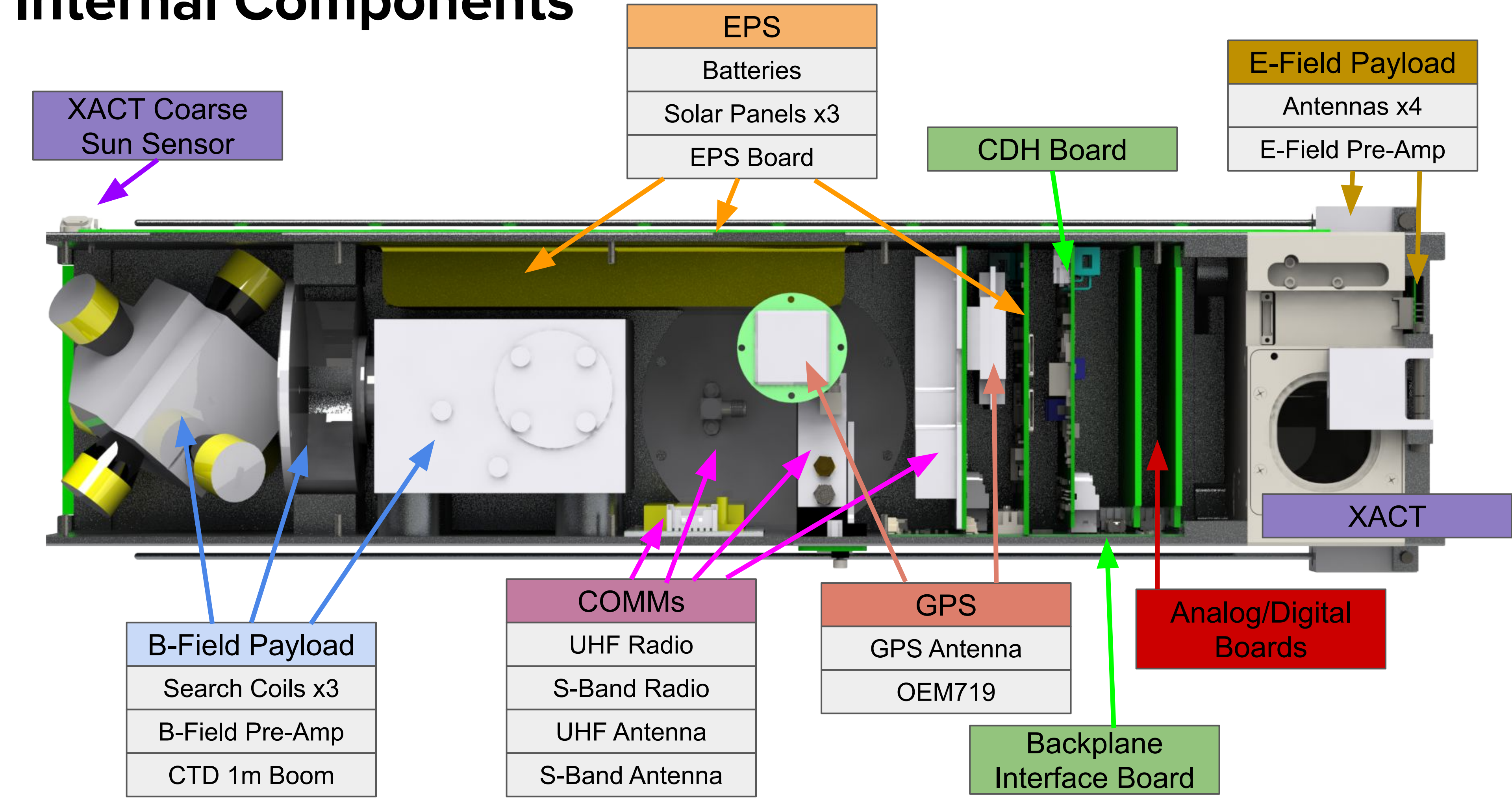


Table 1. Op Amps Selected for TID Investigation

Vendor	Part Number	Application	Supply Voltage	Gain Bandwidth Product	Slew Rate	Max Input Offset Voltage	High Dose Rate Fail Level Rad(Si)	Low Dose Rate Fail Level Rad(Si)
Texas Instruments	OPA656	Wide Bandwidth, FET Input	±5 V	500 MHz	290 V/µs	±1.8 mV	4.7K – 7.7K	>32K
Texas Instruments	TLC2272	Low Noise,Linear CMOS	±5 V	2 MHz	3.6 V/µs	±3.0 mV	12K	12K
Texas Instruments	LMC6062	Precision Micropower CMOS	4.5 to 15V	100 KHz	35 V/ms	350 µV	15K – 25K	15K – 25K
Linear Technology	LTC6081	Low Offset, CMOS	5.5 V	3.5 MHz	1 V/µs	±90 µV	5K	>32K
Linear Technology	LTC1150	High Voltage CMOS	±15 V	2.5 MHz	3 V/ µs	±10 µV	2.5K	5K – 10K
National Semiconductor / Texas Instruments	LMV341	General Purpose w/Shutdown CMOS	5.4 V	1.0 MHz	1 V/µs	±0.025 mV	20K	22K – 27K
Analog Devices	AD8657	Micropower Rail-to-Rail CMOS	18 V	230 KHz	80 V/ms	350 µV	15K – 25K	15K – 25K
Analog Devices	AD8662	Low Noise Precision CMOS	5 to 16V	4.0 MHz	3.5 V/ µs	1 mV	10K- 15K	10K – 15K

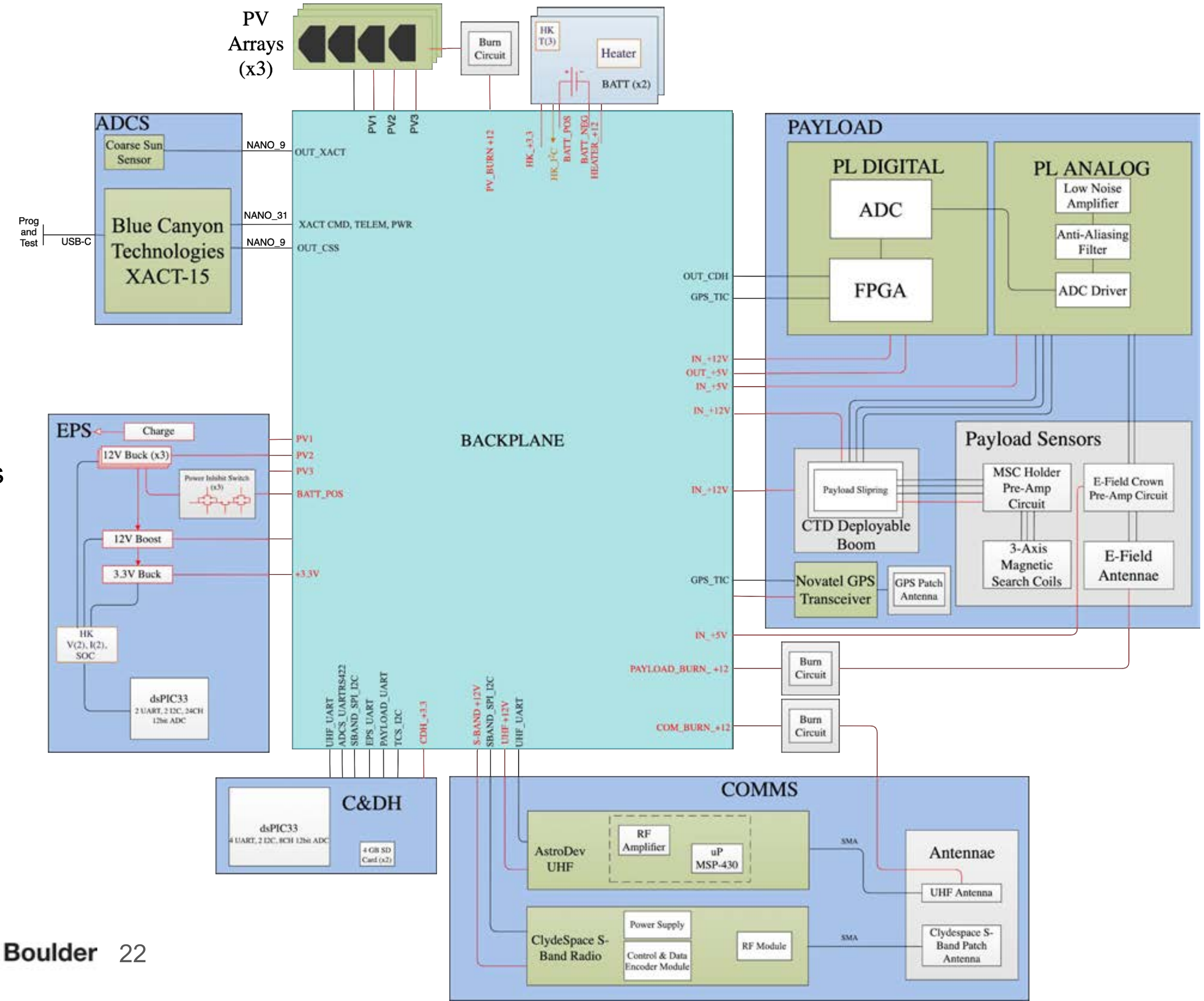
Internal Components



Functional Block Diagram

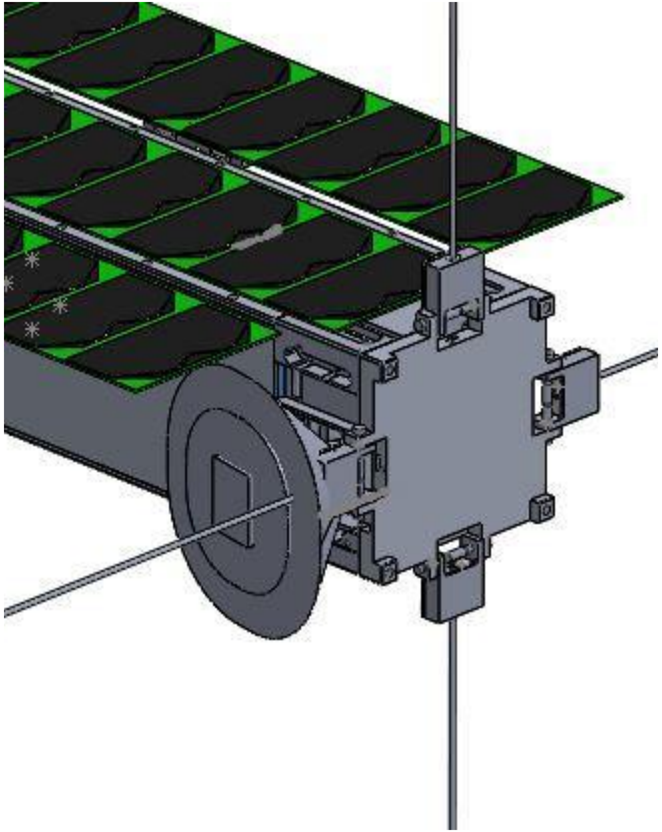
Key takeaways:

- All payload signal processing occurs before signals are passed to CDH, no unprocessed signals are sent through the backplane
- CDH communicates with the payload through the FPGA only, except for HK data
- GPS fed directly to XACT and pulled from XACT HK similarly to COSMO



Antenna Interference

- XACT Star Tracker FOV clear
- Glint-Free keep-out (middle cone) is NOT clear
  - Coating E-field Antennas with DAG213
    - 0.89 absorptivity
    - Low volume resistivity
- Tilting antennas would have incurred large schedule setbacks



"BCT suggestions regarding black coatings do not at all constitute concurrence from BCT that these steps will enable the tracker to function despite glint keep-out violations. LASP shall take ownership of any and all analysis that justifies operating the tracker with the present keep-out violations, as well as any tracker issues potentially caused by glint in the actual flight. BCT will have limited resources available to help solve what may be an impossible problem."

CONOPs and Overview Change Summary

Additions

- Different pointing targets for sunlit and eclipse sides of orbit
  - Requires attitude maneuver planning and scheduling
- Black coating to reduce glint from E-field antennas
- Wire harnesses - SE needs to work with individual subsystems for physical wiring interfaces

Updates

- Updates in mission design fidelity and pointing requirements as data and link budgets increase in fidelity. Lower margins moving forward are expected as uncertainty decreases
- Moved S-Band radio placement based off initial assumptions and understanding of radio radiation patterns

Tracking

- Continue to track budgets through testing and final design phases

Instrumentation

Riley / Keith / Kyle

Science Traceability Matrix

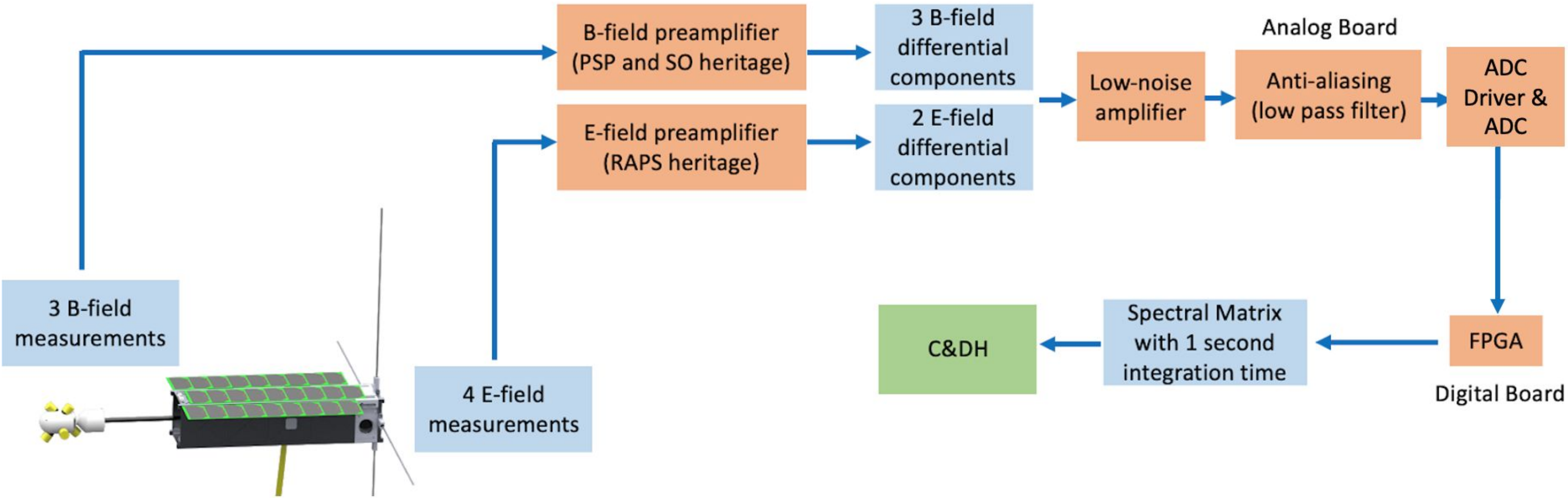
NASA Science Goal	Investigation Science Objectives	Science Measurement Requirements		Instrument Performance				Mission Functional Requirements
		Physical Parameters	Observable	Parameter		Requirement	Projected	
NASA 2013 Solar and Space Physics Decadal Survey, Priority #2: Determine the dynamics and coupling of Earth's magnetosphere, ionosphere, and atmosphere and their response to solar and terrestrial inputs	What is the average electromagnetic energy input into the space environment by lightning?	VLF wave power and k-vectors	VLF wave amplitude and phase in E and B components	E-field	Minimum sensitivity	10^-6 V/m/rt-Hz	10^-6 V/m/rt-Hz	One-year mission
					SFDR	50dB	> 50dB	
					Frequency range	0.3-40 kHz	0.3-40 kHz	>50 deg inclination
	What is the spectrum of VLF wave energy above the ionosphere in the 0.3—40 kHz frequency range?	VLF wave spectral energy density	VLF wave spectra in E and B components		Frequency resolution	10%	8.5%	
					Time resolution	1 sec	1 sec	Attitude knowledge within 1 degree accuracy
				B-field	Minimum sensitivity	100 fT/rt-Hz	20 fT/rt-Hz	
NASA 2014 Science Plan, Heliophysics science goals: i) Explore the physical processes in the space environment from the Sun to the Earth and throughout the solar system					SFDR	50dB	> 50dB	On-board FFT engine
	What is the transmission transfer function of the ionosphere for VLF energy, and how does it vary in space and time?	VLF wave power and spectrum	VLF wave amplitude and spectra above VLF transmitters		Frequency range	0.3-40 kHz	0.3-40 kHz	
					Frequency resolution	10%	8.5%	Fast survey mode
					Time resolution	1 sec	1 sec	

Data Budget

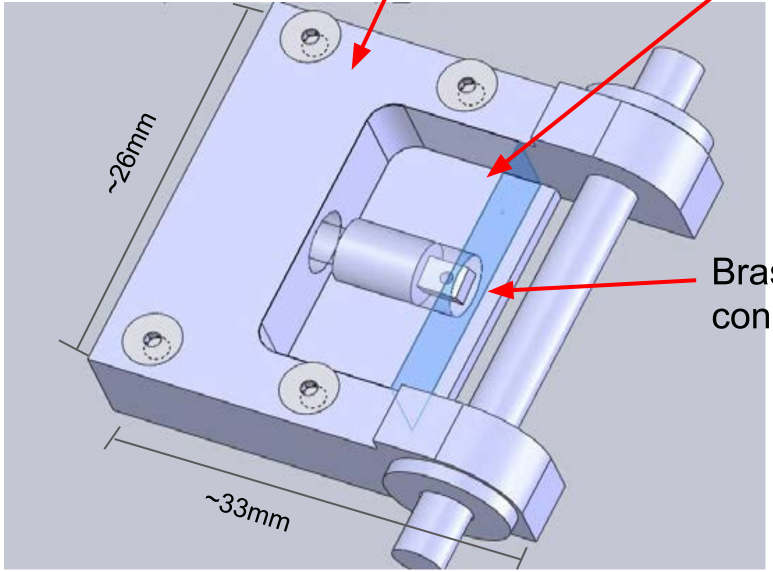
FFT Frequency bins	67	bins
Time resolution (spectra/sec)	1	Hz
Spectral Matrix:		
Number of values: diagonal	5	values
Bit depth (diagonal)	8	bits
Number of values: off-diagonal	20	10 complex numbers
Bit depth (off-diagonal)	12	bits
Bits per spectral matrix	**280**	bits
Bits for time-tag	**64**	bits
Data production rate	**18824**	bits/sec

Packet Headers/day	148901	bits/day
Recording time per day	86400	sec
Total data produced per day	**193.899**	**MB/day**
Ground station coverage per day	15.16	min
(sec)	909.6	sec
Downlink rate	2.10E+06	bits/sec
Data downlink capability per day	**227.71**	**MB/day**
Margin	**14.848**	**%**

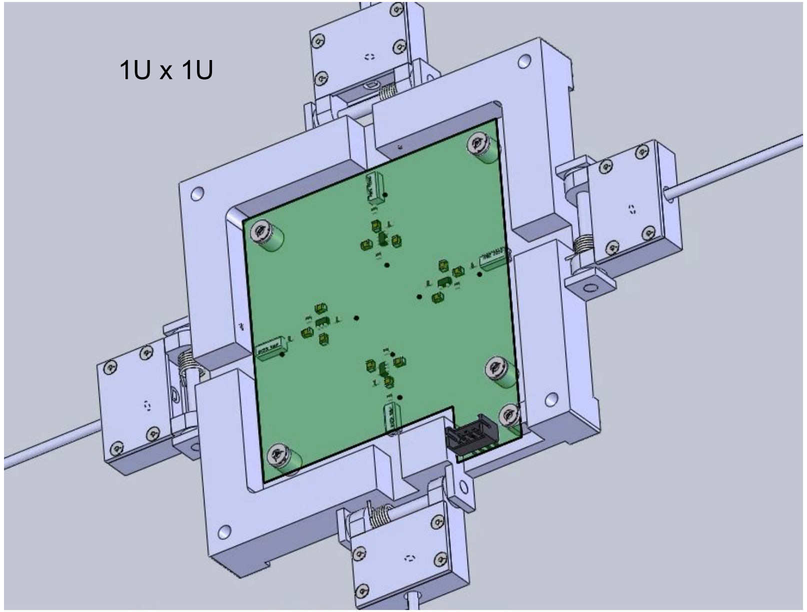
Instrumentation



E-Field Antennas - Overview



E-field crown

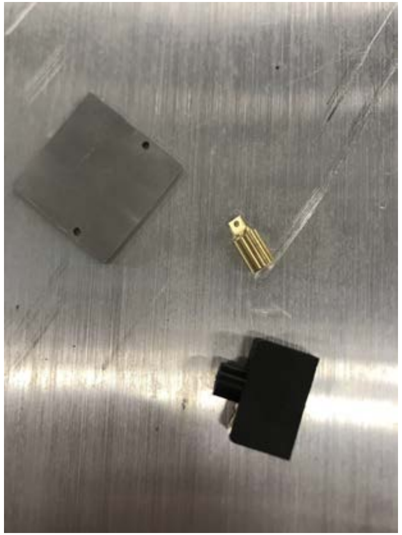


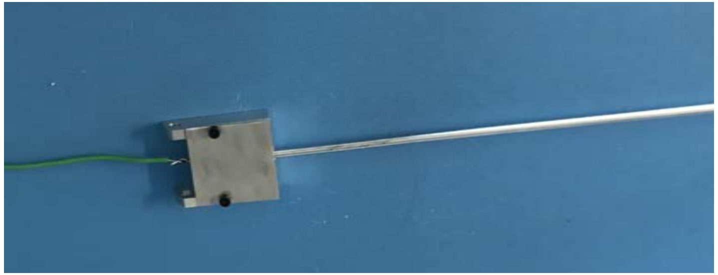
E-Field Antennas - Key Requirements

Req.	Description	Reasoning
SCI-1.1	CANVAS E-field antennas will be designed to have low capacitance (<10pF)	CANVAS shall measure electric fields between 0.3 Hz and 40 kHz (so do not want antenna capacitance to introduce a low-pass characteristic that rolls off prior to 40 kHz)
SCI-1.5	CANVAS E-field antennas will have a spring-actuated deployment mechanism.	CANVAS shall measure electric fields in the band of interest with sensitivity, SFDR, flatness, and orthogonality requirements

E-Field Antennas - System Status

- Design based on RAPS work
  - Adjusted for CANVAS size
  - Ease of manufacturing and ease of assembly
  - Low capacitance
- Prototype 1 manufactured with preliminary testing complete

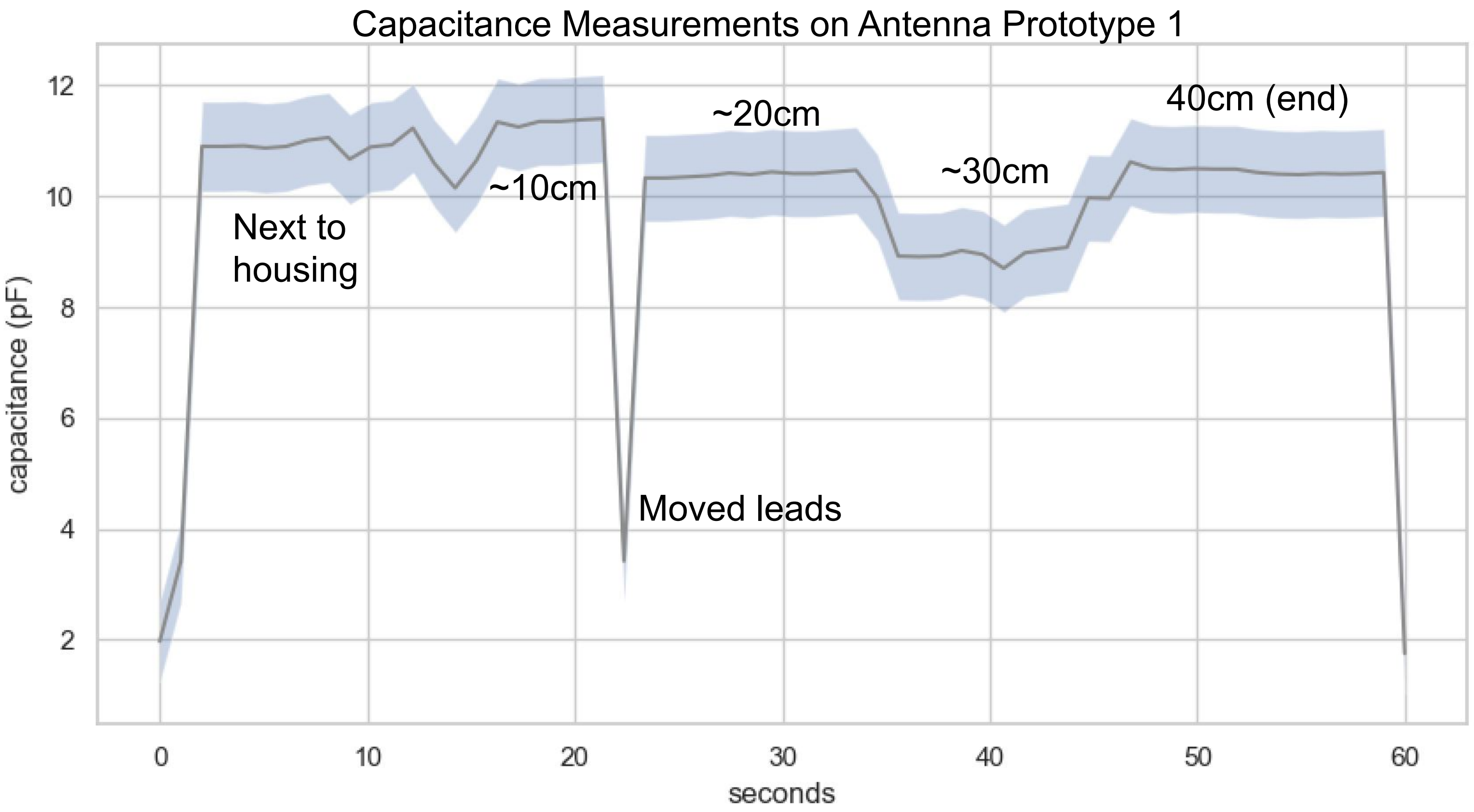




E-Field Antennas - System Status

Recorded capacitance reading for 1 minute, moving down the length of the antenna starting at the housing

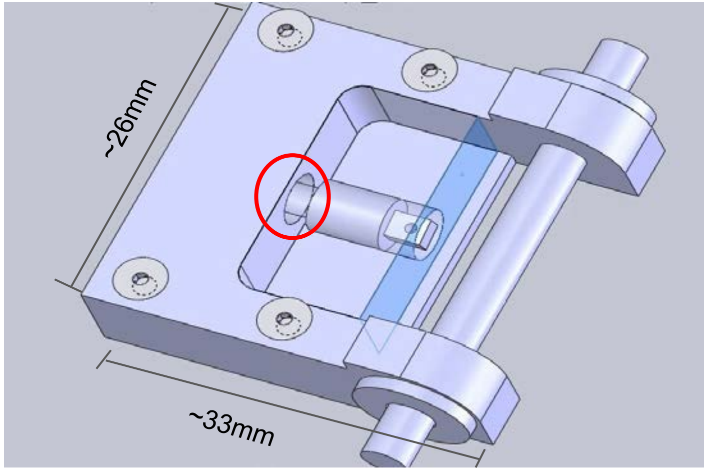
Antenna capacitance to housing between 8-12pF



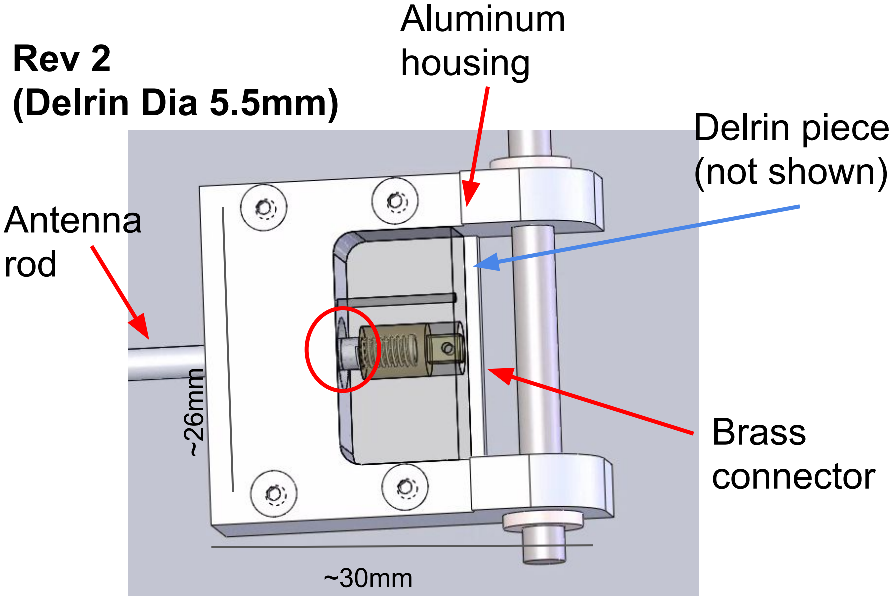
E-Field Antennas - System Status

- Prototype 1 manufacturing led to design changes reflected in revision 2
  - Increased ease of manufacturing by threading antenna rod
    - Loctite 3888 will be used to secure antenna with <0.001 Ohm/cm^3 volume resistivity
  - Decreased diameter of delrin piece to further reduce capacitance

Prototype 1
(Delrin Dia = 5mm)

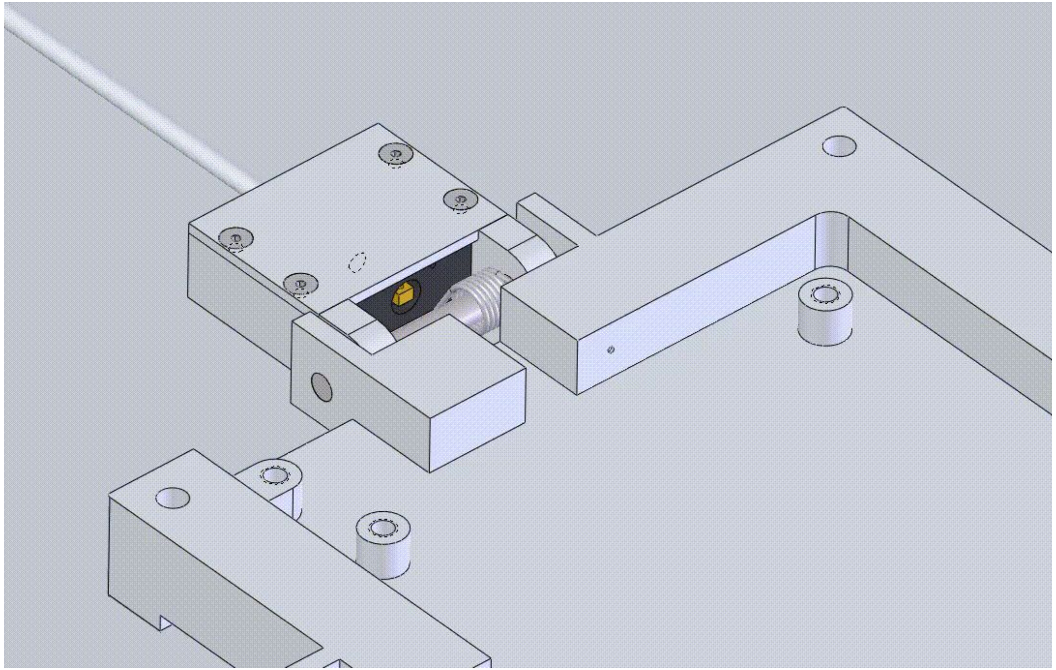


Rev 2
(Delrin Dia 5.5mm)



E-Field Antennas - System Status

- Prototype 2 revised assembly plan
    - Includes properly defined fits and tolerances
        - Can press-fit hinge pin into one side of the arms to secure entire assembly
    - Under review by Nate in the AERO Machine Shop



E-Field Antennas - Next Steps

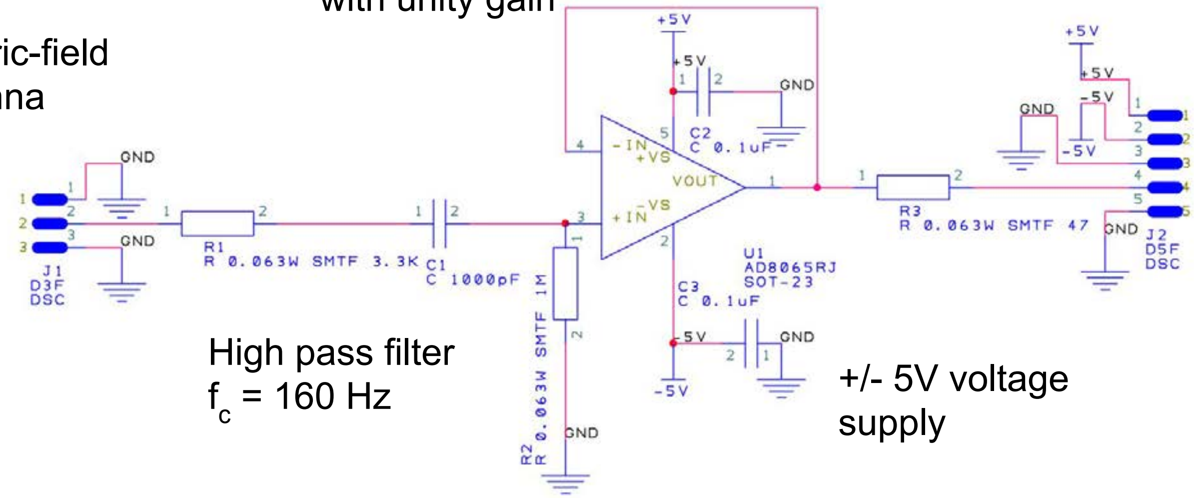
- Manufacture revision 2 of E-field antenna assembly in AERO machine shop
  - Update and use assembly plan document to assemble rev 2 prototype
  - Estimated to accomplish early Fall semester
- Repeat capacitance testing on revision 2
  - Plan for capacitance testing with full mock-up of the spacecraft
  - Perform pre- and post-DAG213 tests for capacitance
  - Goal: accomplish this upcoming semester with CANVAS sized aluminum body
- Revise sensitivity test plan and perform sensitivity analysis (discussion following E-field preamp discussion)
  - Estimated to accomplish early Fall semester with updated test plans
- Prepare for spring storage test on revision 2
  - Long term storage of spring assembly in stowed position to confirm 90 degree deployment
  - Storage for at least 6 months
  - Planning to start test with rev 2.
- Full signal path test of payload prior to spacecraft integration and testing

E-Field Preamp - Overview

- Using RAPS design buffer preamplifier
- V2 design completed

Input signal from electric-field antenna

AD8065 op amp with unity gain



High pass filter
f_c = 160 Hz

+/- 5V voltage supply

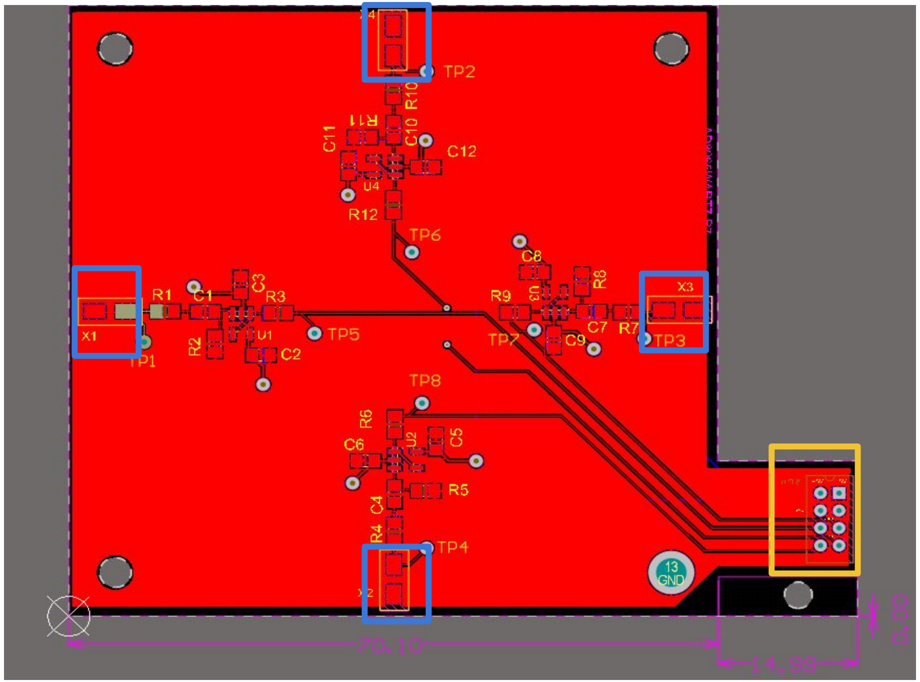
Output signal to analog board

E-Field Preamp Key Requirements

Req.	Description	Reasoning
SCI-1.2	Measure E fields with sensitivity less than 10^-6 V/m/rt-Hz in the band of interest	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-1.3	Measure E fields with a minimum SFDR of 50 dB above the sensitivity requirement	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-1.4	Have a uniform gain within 3 dB across the frequency band of interest	Uniform gain allows for uniformly amplified data for each frequency band

E-Field Preamp Status

- Ordered, populated, and tested PCB v2
  - Improved layout and routing
  - Mechanical interfacing with the E-field Crown

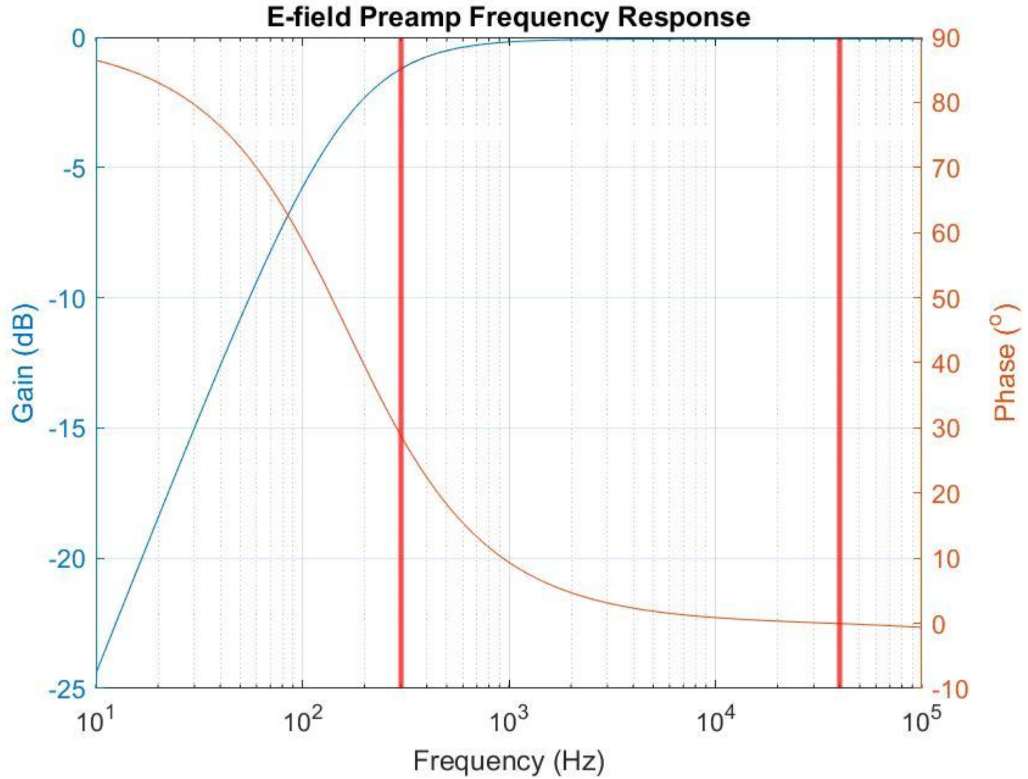


4 signal input into
4 identical channels

2 differential
signals output

E-Field Preamp Status- Frequency Response

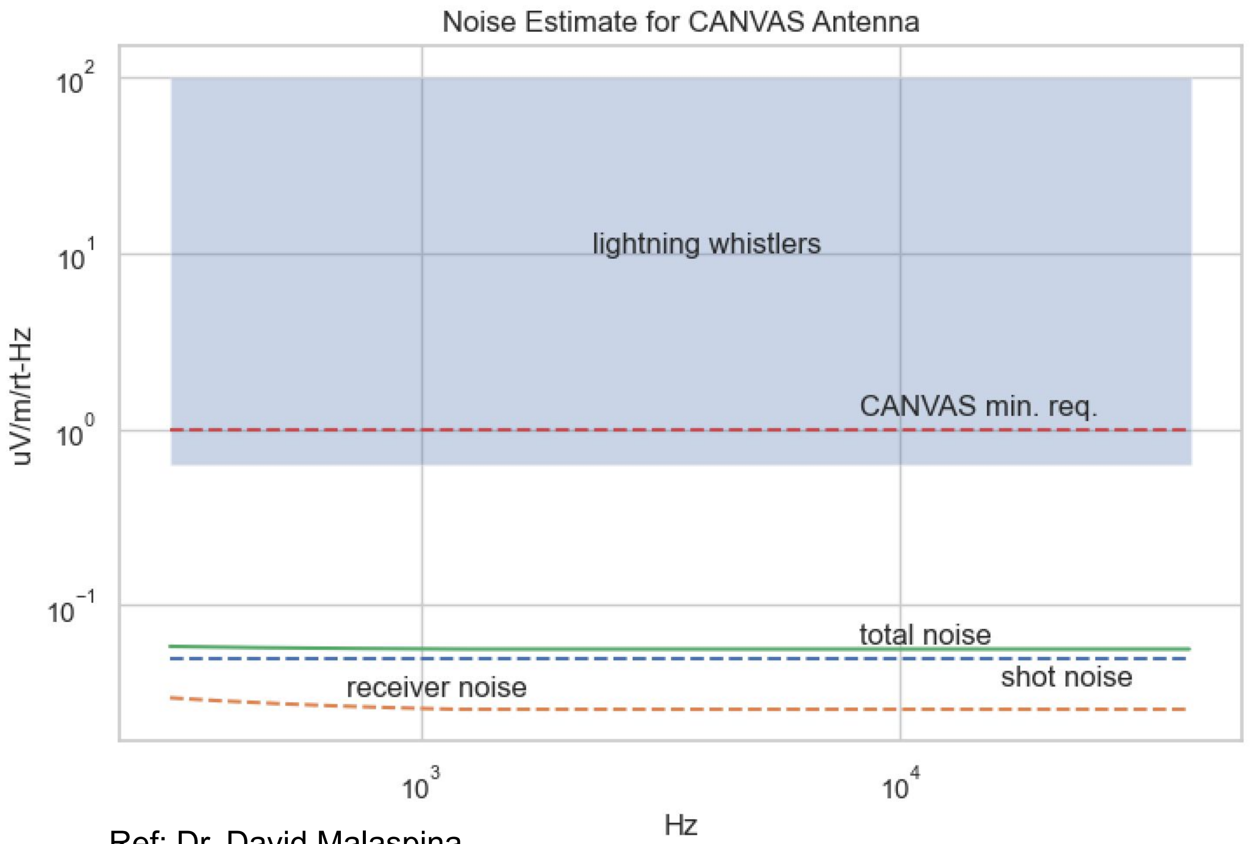
SCI-1.4:
Have a uniform gain within 3 dB across the frequency band of interest



300 Hz **40 kHz**

E-Field Preamp- Sensitivity Testing w/ Antenna rev 1

SCI-1.2:
Measure E fields with sensitivity less than 10^-6 V/m/rt-Hz in the band of interest



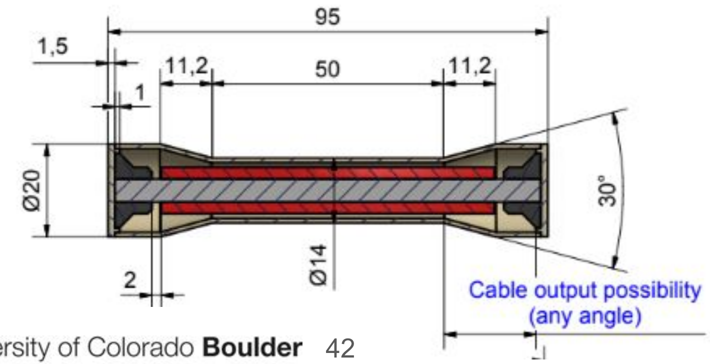
Ref: Dr. David Malaspina

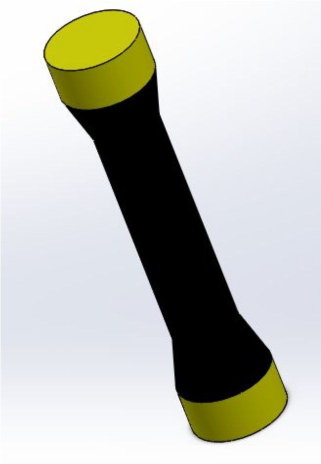
E-Field Preamp Next Steps

- Test the sensitivity of the E-field Preamp to verify SCI-1.2
  - Revise test plan and test setup
  - Estimated: September 2020
- Verify connector selections are mechanically stable (call suppliers, preliminary vibe testing)
  - Estimated: September 2020
- Detail mechanical interfaces to the analog board
  - Closer look at routing the wires through the spacecraft to the Analog board
  - Estimated: September/October 2020
- Full signal path test of payload prior to spacecraft integration and testing
  - Estimated: end of Fall semester 2020
- Detailed plans for Flight assembly boards
  - Estimated: Spring 2021

3-Axis Search Coils

- Designed and built by CNRS, based on designs from DEMETER, TARANIS, PSP etc.
- Coils of wire around a ferromagnetic core
- Using principle of Faraday's law of induction:
    - Varying magnetic flux from VLF waves will induce a voltage in coils
    - Transfer function allows us to back out the original magnetic flux
    - 3 search coils in mutually orthogonal directions allows for measurements in 3 directions
    - Deployed on end of 1 meter long boom: CTD boom

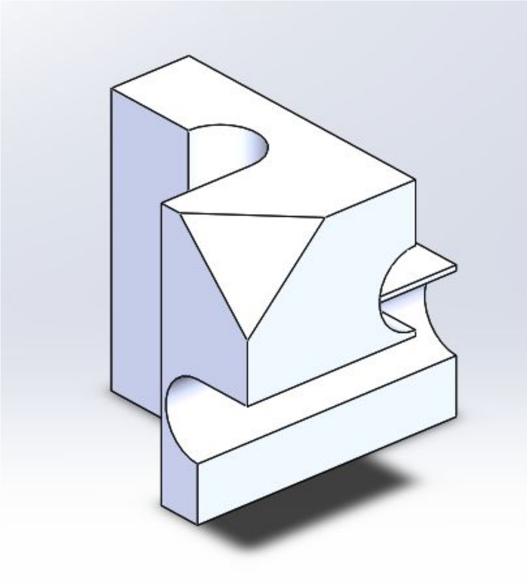


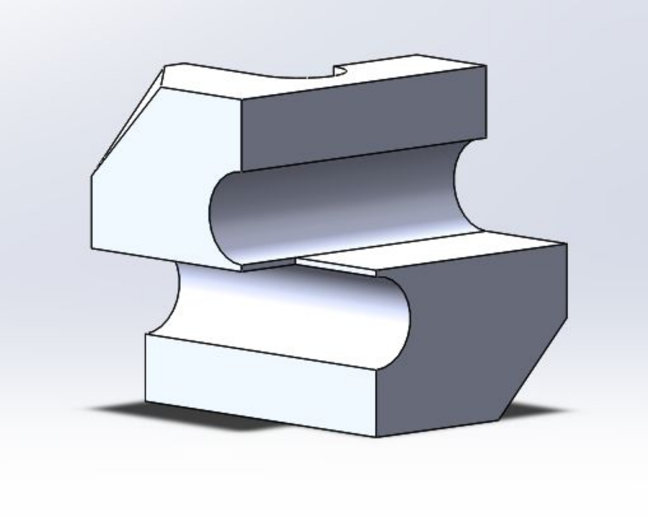


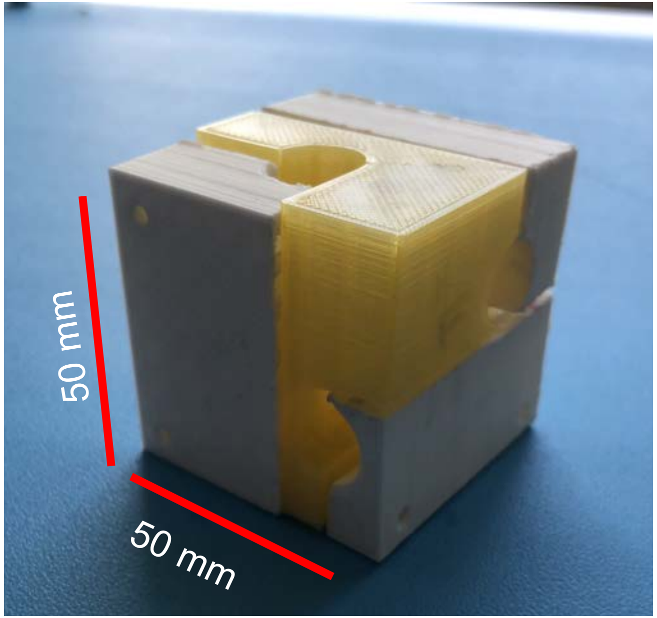
B-Field Holder - Key Requirements

Req.	Description	Reasoning
SCI-2.5	CANVAS shall measure orthogonal Magnetic field components to within 5 degrees	B-Field components shall be known relative to the the S/C bus in order to be known within an inertial frame
SCI-2.2	CANVAS shall measure magnetic fields with sensitivity less than 10^-4 nT/rt-Hz in the band of interest	Observed whistler wave amplitudes from previous missions impose reqs. for sensitivity. The holder shall be made out of a non-conductive material as to not interfere with magnetic field measurements

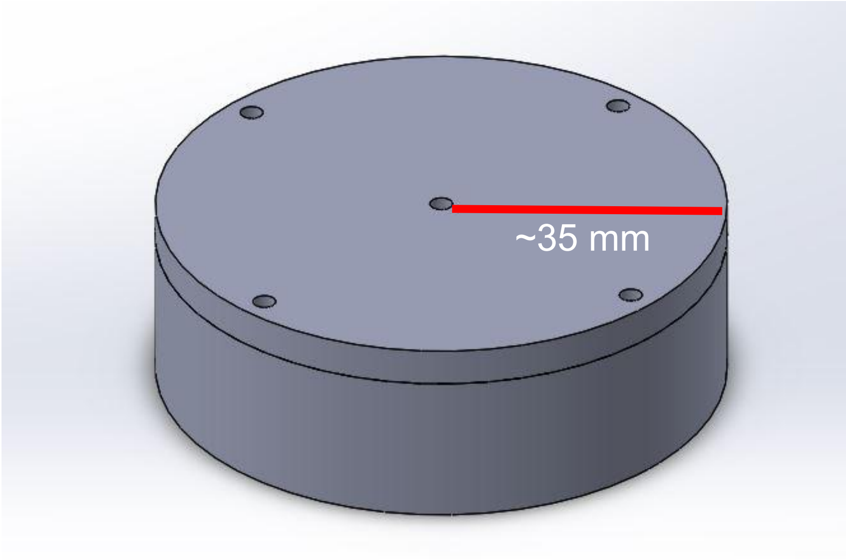
B-Field Holder - Status

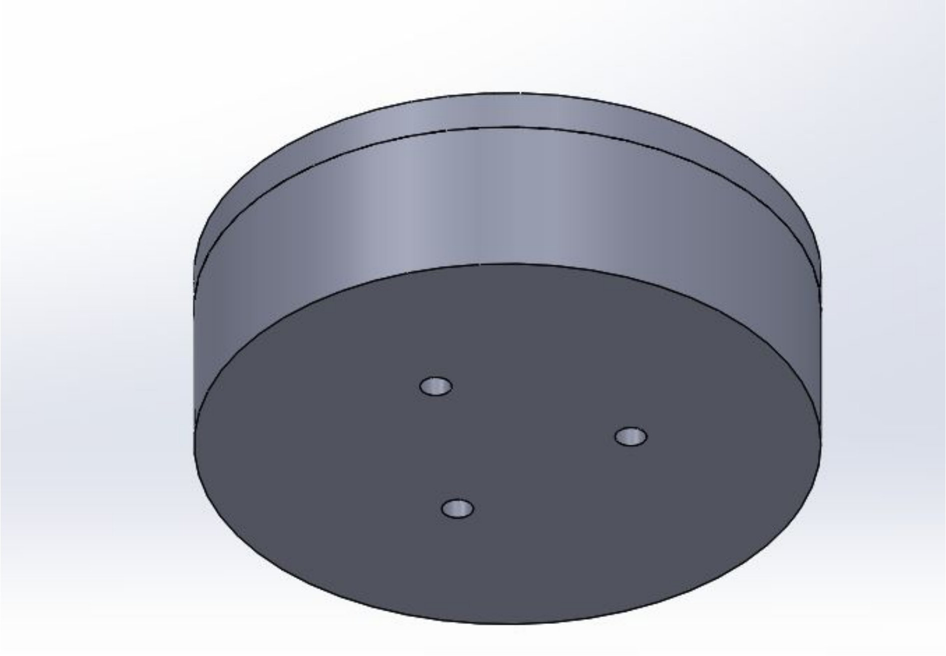




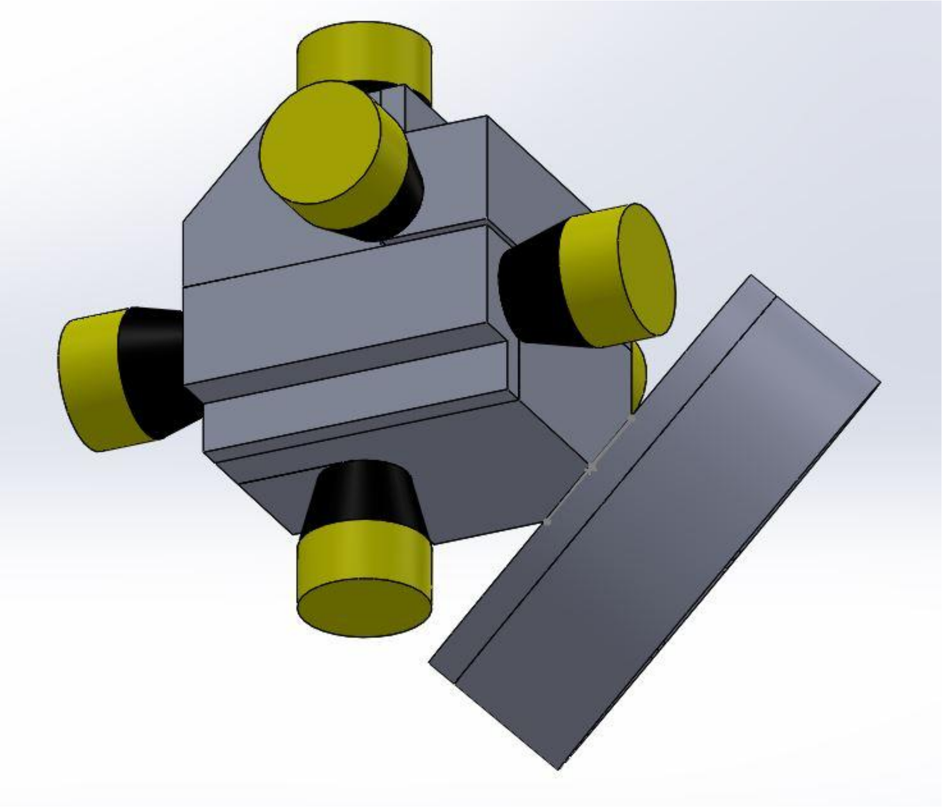


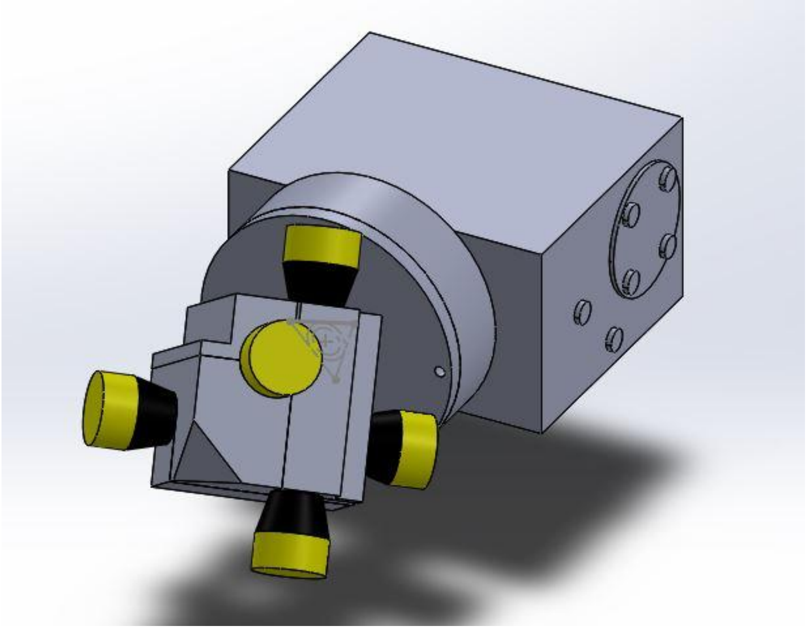
B-Field Holder - Status





B-Field Holder - Status



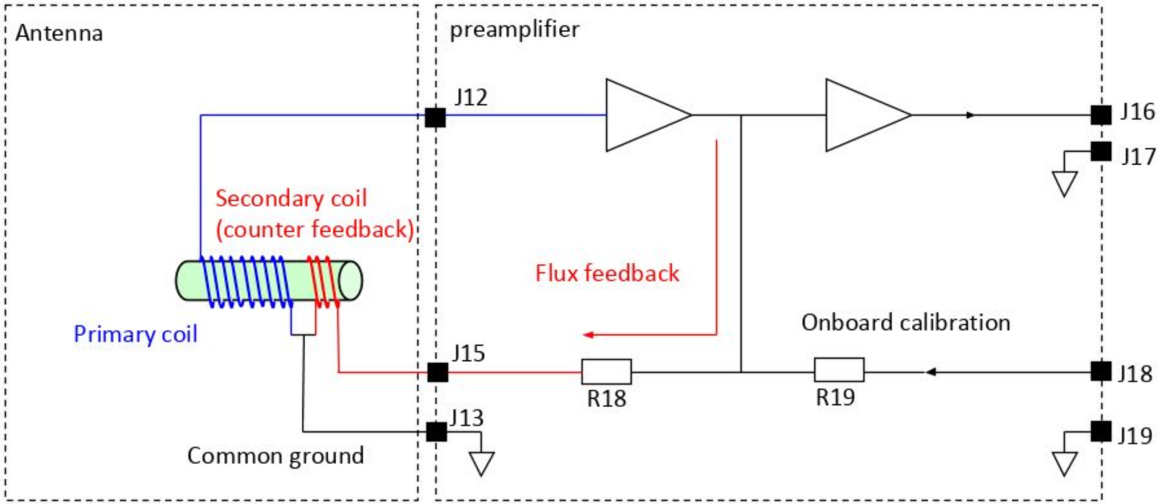


B-Field Holder - Next Steps

- Finalize material selection (currently selected PEEK)
  - PEEK selection due to high temperature tolerance, low conductivity
  - May need to cover with UV protection
- Increase fidelity of stabilizer design
  - Estimated early Fall 2020
- Detail wire routing to the preamp and from preamp to boom root
- Determine mechanical interfacing to boom root and preamp
  - Estimated Sept/Octi Fall 2020
- 3D-print prototype and test fit with search coils
  - Expect the search coils to arrive ~September from France
- Detailed manufacturing and assembly plans
- **Cross talk analysis with preamplifier**
  - Estimated Oct/Nov 2020

B-Field Preamp - Overview

- Using circuit with heritage from DEMETER, TARANIS, PSP, SO
    - Adjusting frequency range and voltage supply

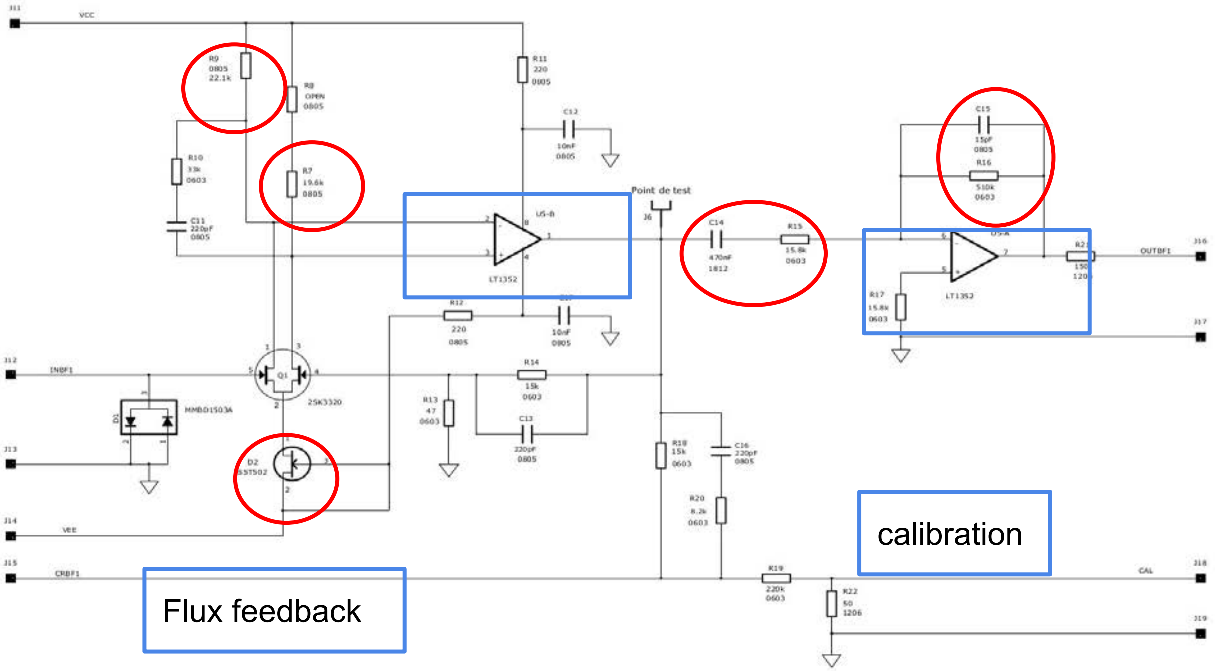


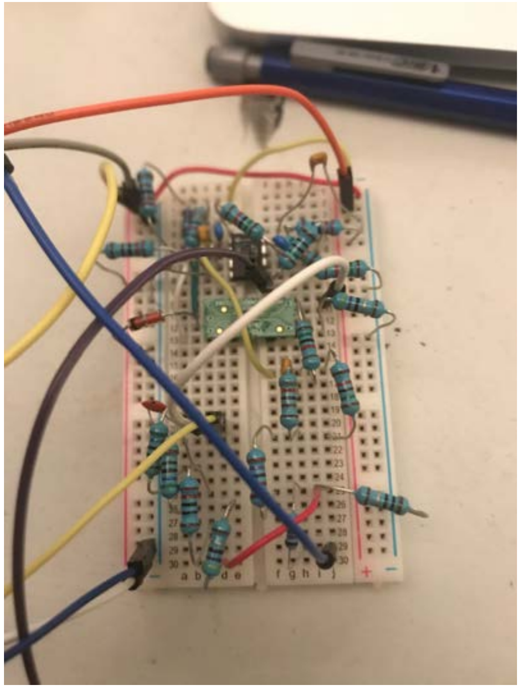
B-Field Pre-Amp - Key Requirements

Req.	Description	Reasoning
SCI-2.2	Measure B fields with sensitivity less than 10^-4 nT/rt-Hz in the band of interest	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-2.3	Measure B fields with a minimum SFDR of 50 dB above the sensitivity requirement	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-2.4	Have a uniform gain within 3 dB across the frequency band of interest	Uniform gain allows for uniformly amplified data for each frequency band

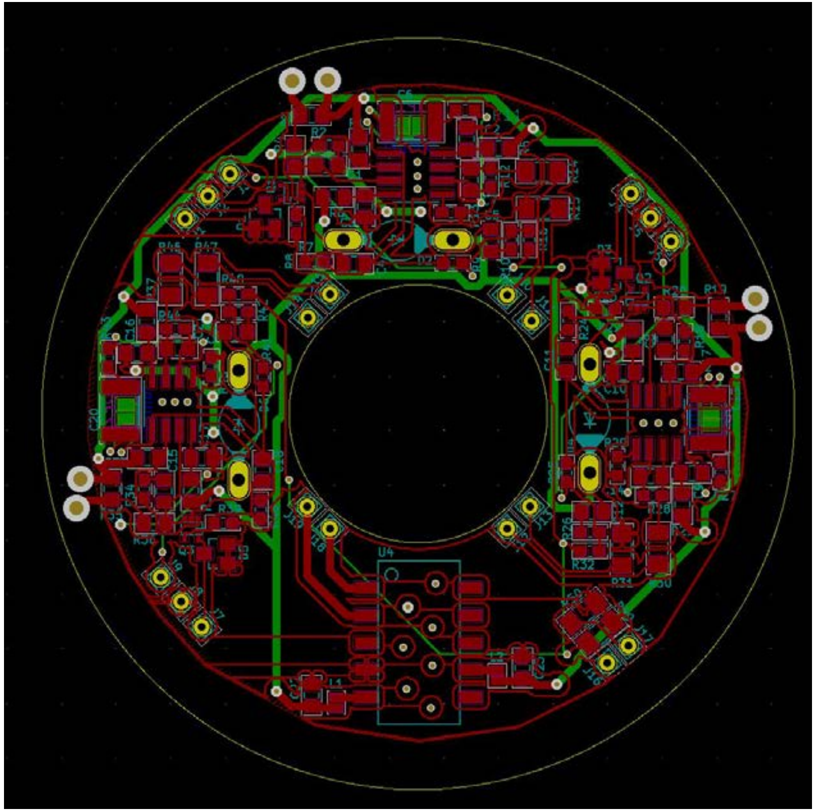
B-Field Preamp - Status

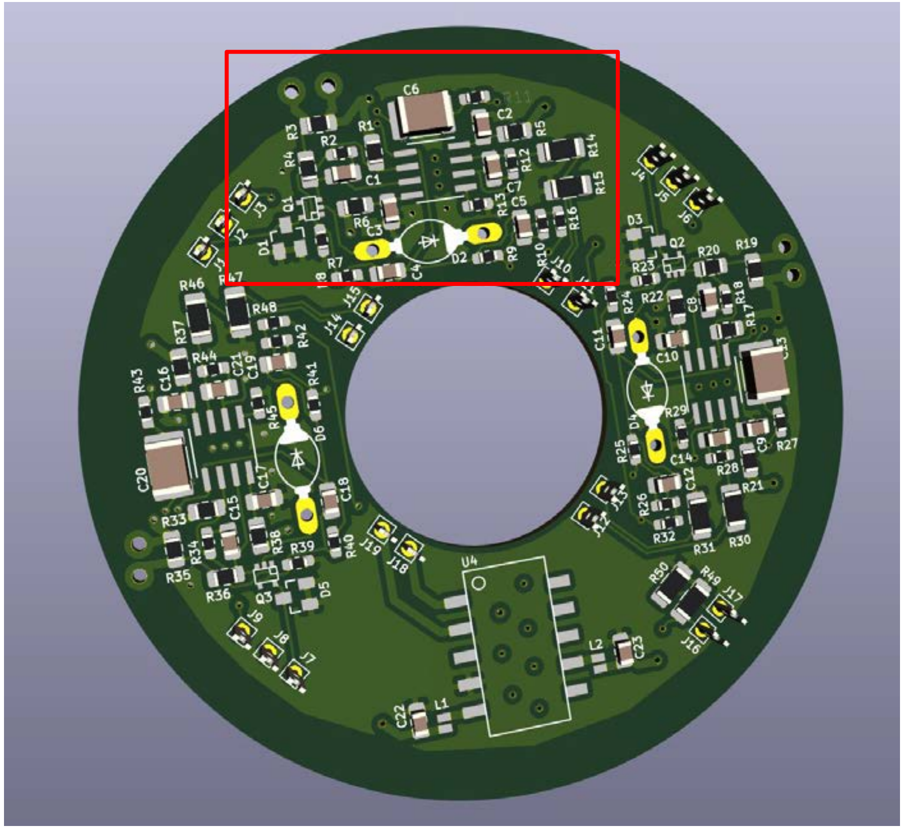
- Adjusted frequency cutoff and voltage supply circuit



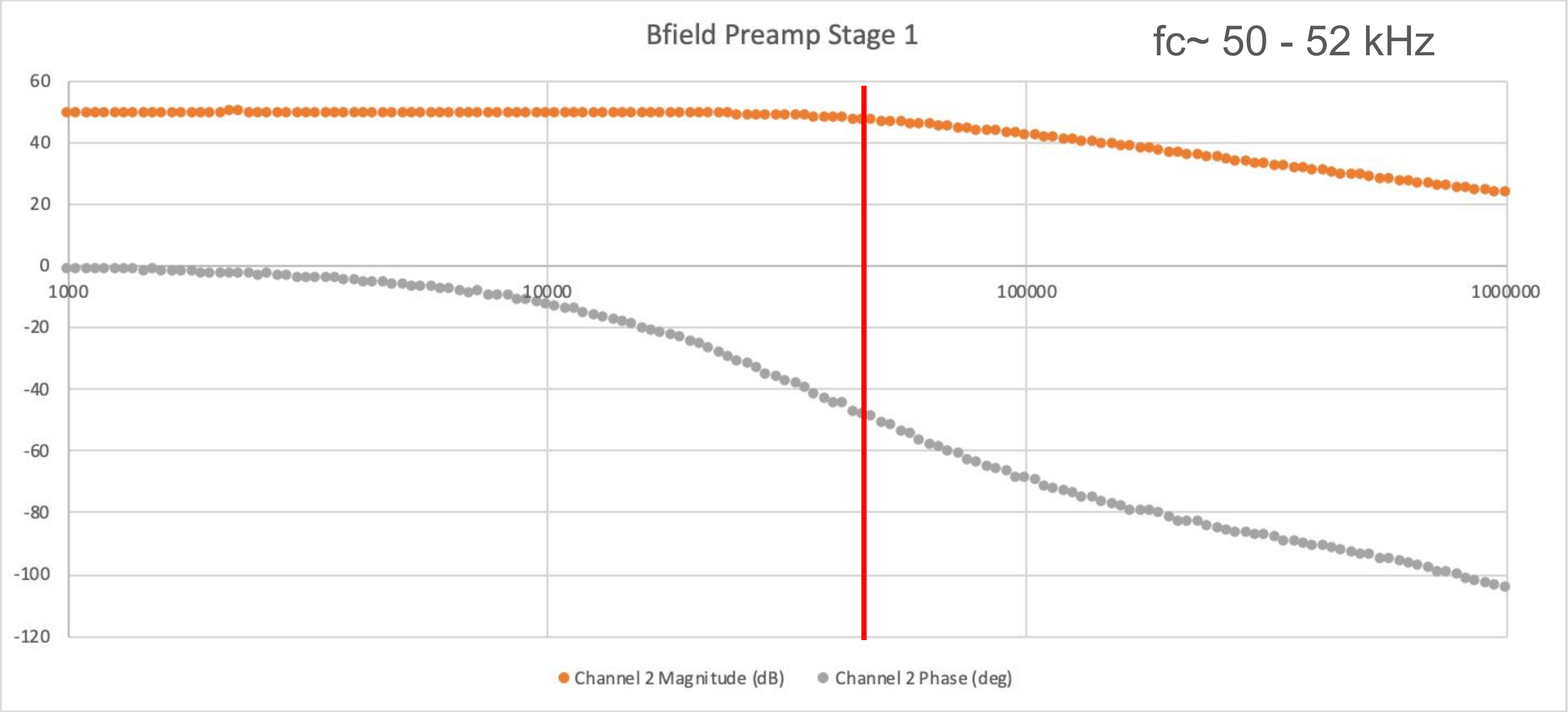


B-Field Preamp - Status

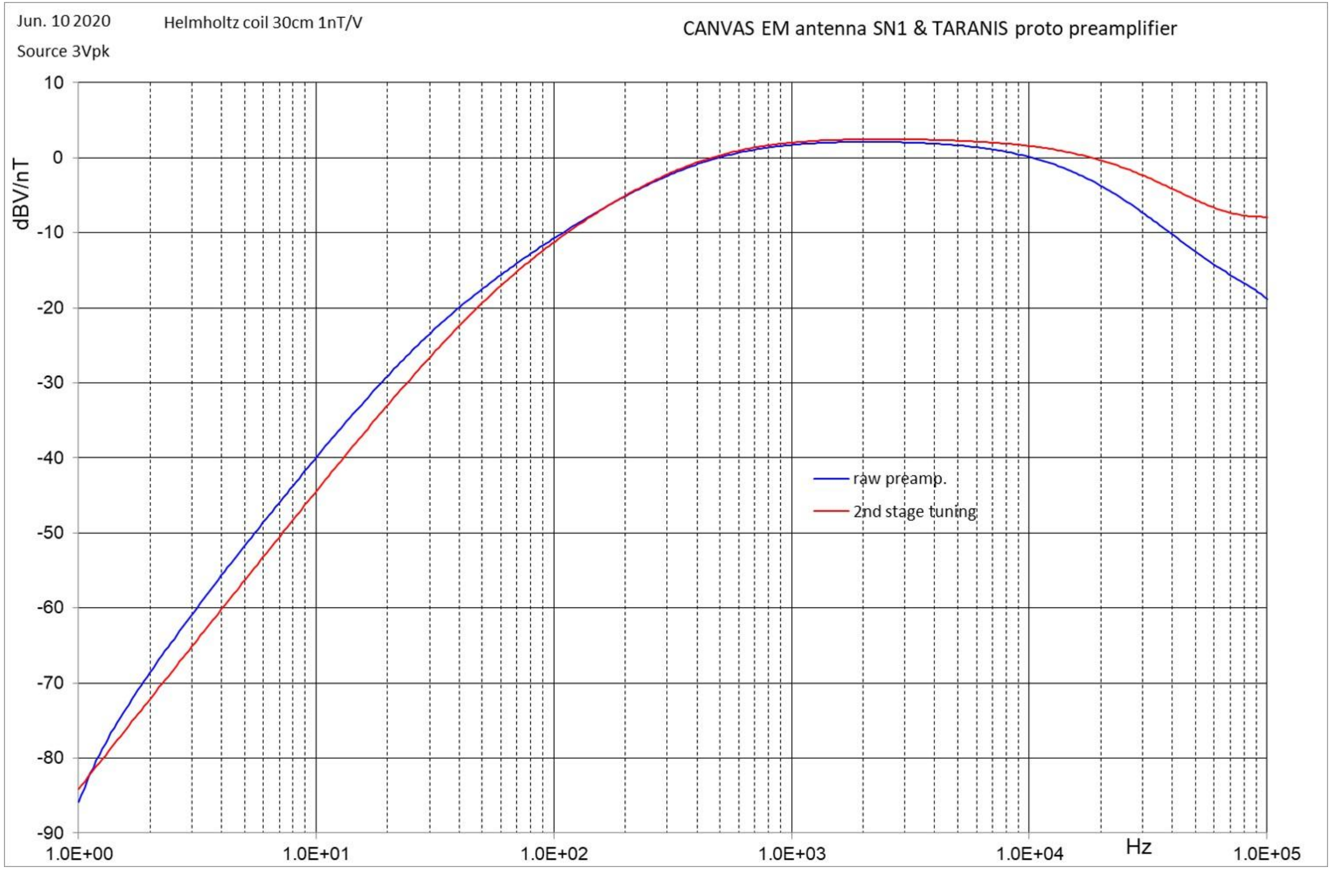




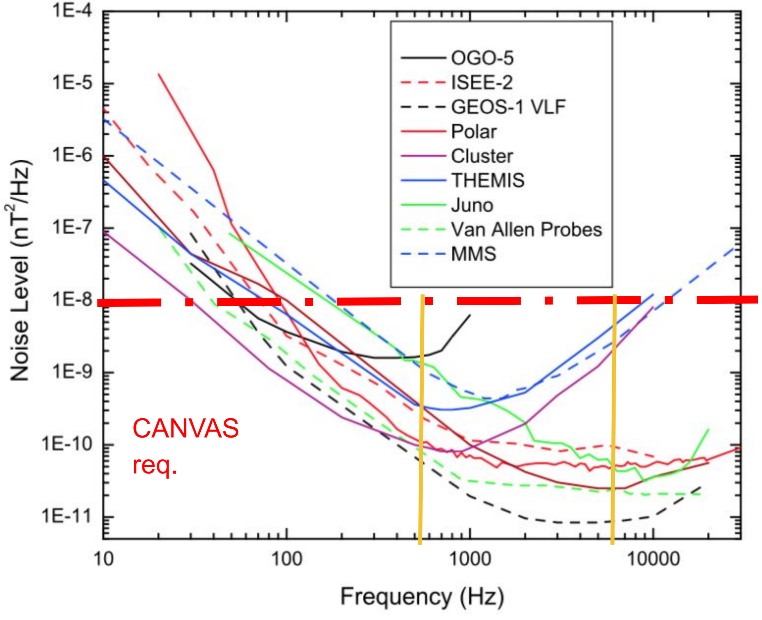
B-Field Preamp - Status



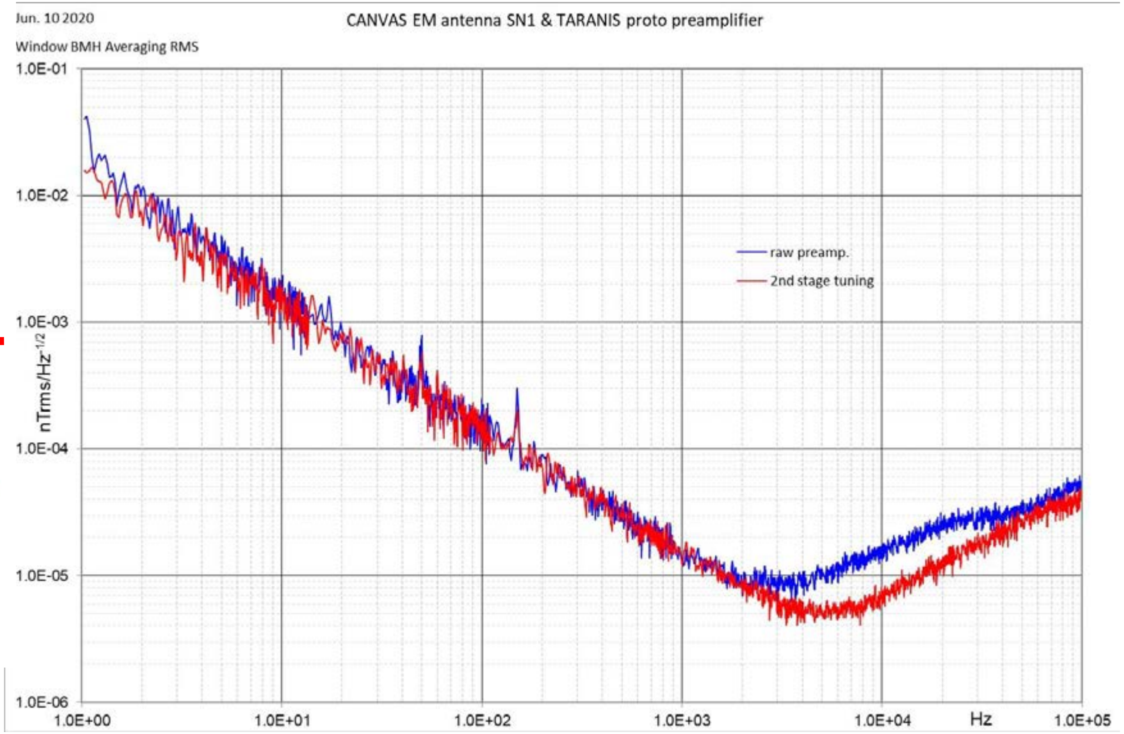
B-Field Preamp - Status



B-Field Preamp - Status



Hospodarsky, et. al.

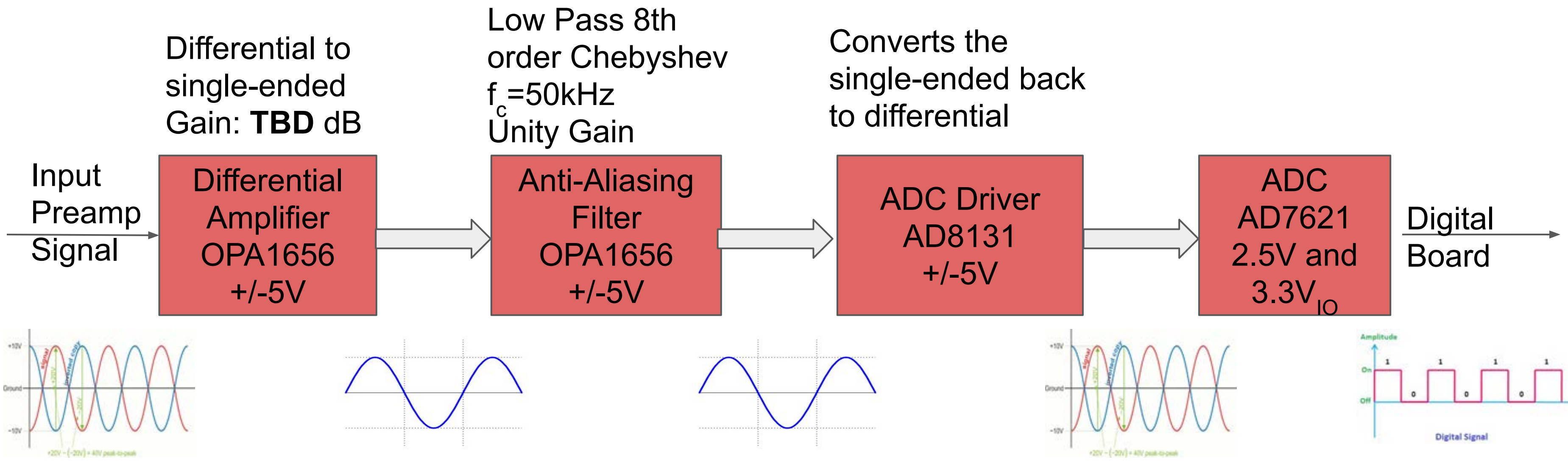


B-Field Preamp - Next Steps

- Incorporate revisions from Guillaume into rev 2 as a breadboard
  - Estimated: September 2020
- Select improved DC/DC converter with LDO/something similar for noise reduction
  - Estimated: September/October 2020
- Detail mechanical interfaces to holder and electrical interfacing to search coils and analog board
  - Estimated: September/October 2020
  - Requires a closer look at routing through the B-field holder
  - Requires a closer look at routing from the preamp to the analog board through the SC
- Determine transfer function of search coils to size additional gain needed at the analog board
  - Estimated: September/October 2020
- Order and test rev 2 for frequency response and sensitivity

Analog Receiver Board - Overview

- Functional Overview (one of 5 channels: 2E-field, 3B-field)
    - Based on RAPS design
    - Two DC-DC Converter
        - 12V to +/-5V
        - 12V to 2.5V

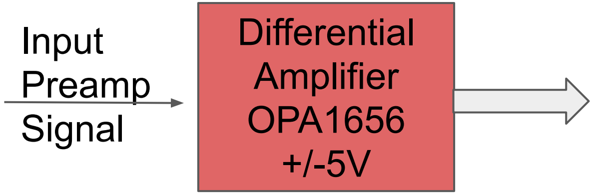


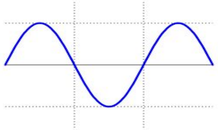
Analog Receiver Board Key Requirements

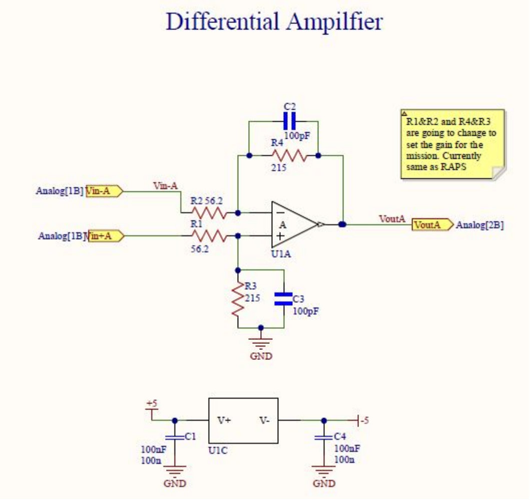
Req.	Description	Reasoning
SCI-1.1 **SCI-2.1**	CANVAS shall measure E & B fields between 0.3 kHz and 40 kHz	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-1.3 **SCI-2.3**	CANVAS shall measure E & B fields with a minimum SFDR of 50 dB above the sensitivity requirement	Observed whistler wave amplitudes from previous missions (DEMETER) impose reqs for sensitivity and SFDR
SCI-1.4 **SCI-2.4**	CANVAS shall have a uniform gain within 3 dB across the frequency band of interest	Uniform gain allows for uniformly amplified data for each frequency band

Analog Board - Status- Differential Amplifier

- Differential Amplifier
  - Uses RAPS Design
  - Op Amp: OPA1656
- Gains will be decided based on literature and ADC input range
- Gain changes with the ratio of R4 and R2
- Gain will be different for the E-field and B-field signals
  - Currently estimating E-field will need ~100x and B-field will need ~10x (after preamp)







Analog Receiver Board - System Status

- Anti-Aliasing Filter design drivers:
- Uniform gain (unity) within 1.5dB
- -60dB stopband attenuation @ 88kHz
- Space and power saving

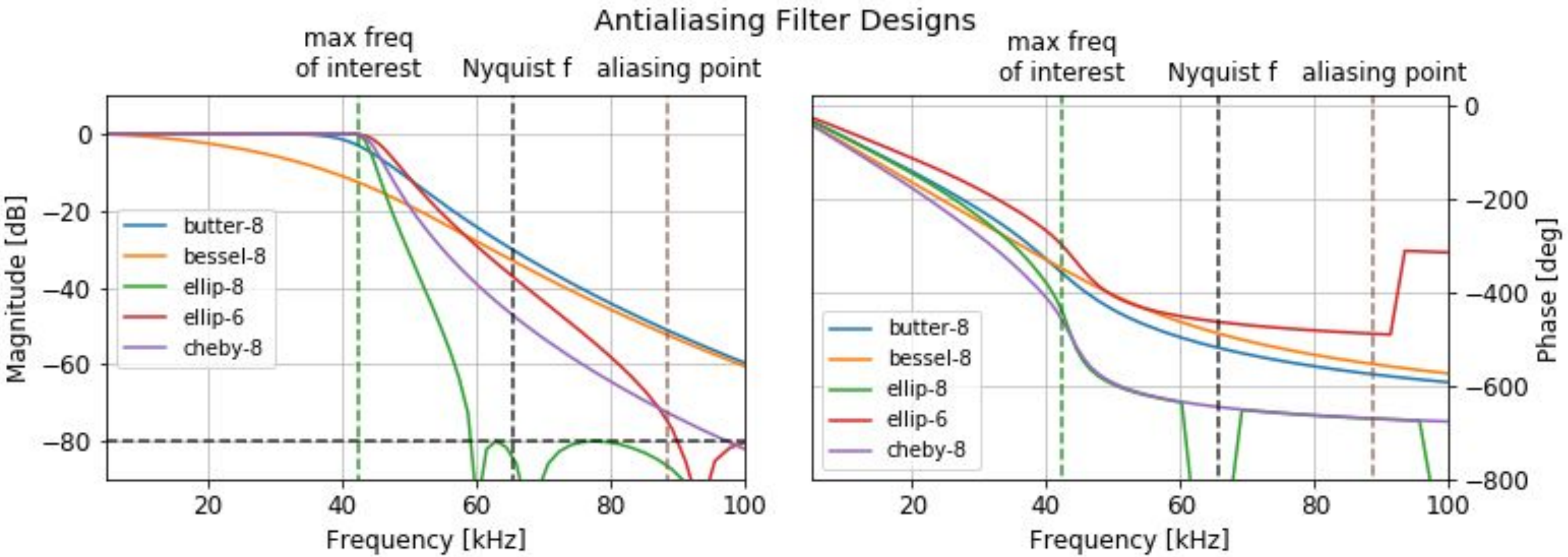
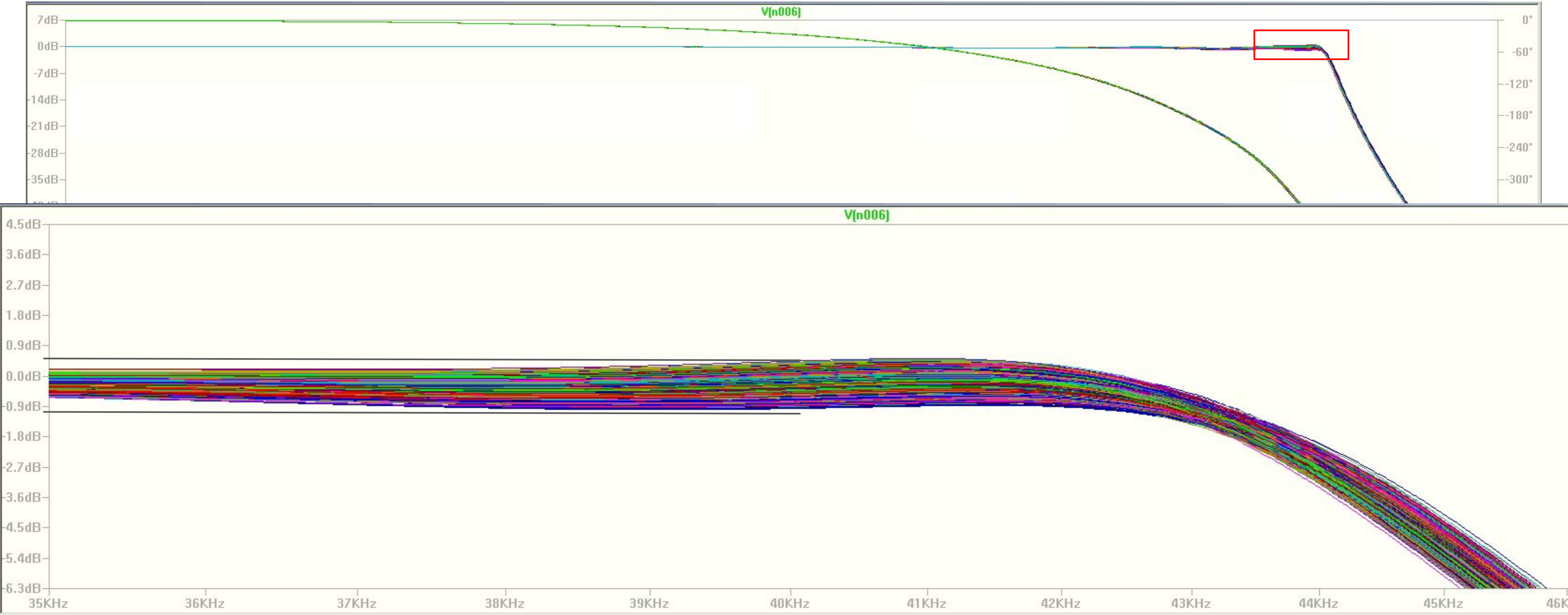


Figure credit: Dr. Austin Sousa, 2020

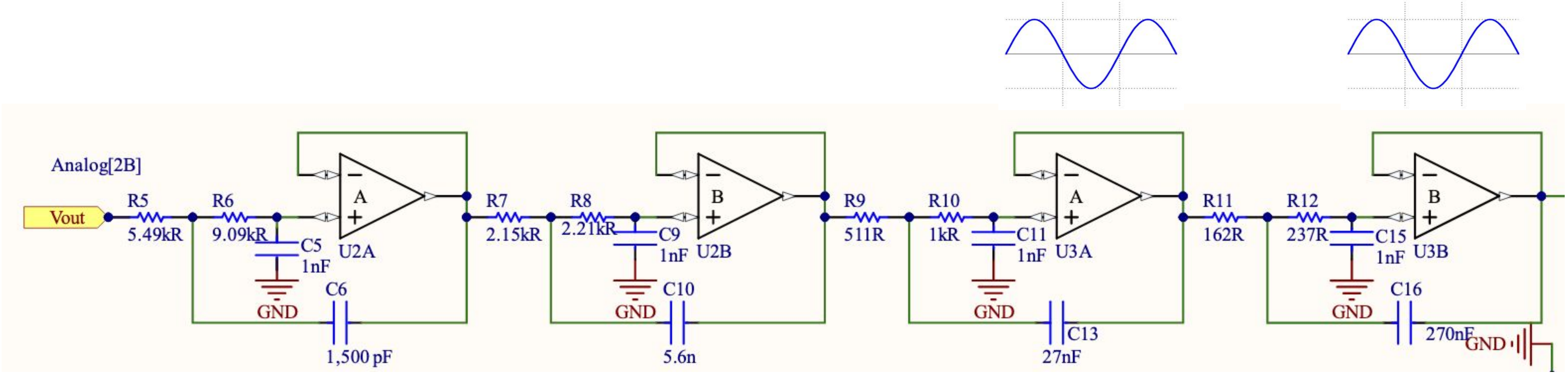
Analog Receiver Board - System Status

- Anti-Aliasing Filter: 8th order Chebyshev design



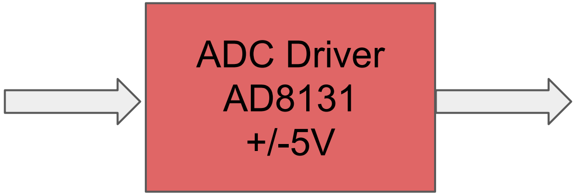
Analog Receiver Board - System Status

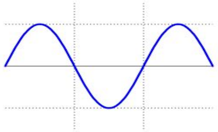
- Anti-Aliasing Filter: 8th order Chebyshev design

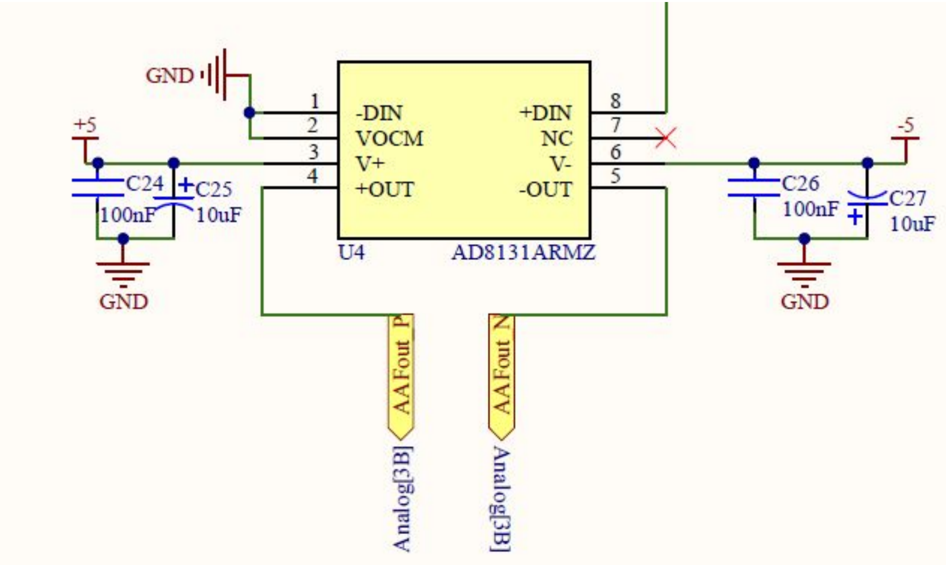


Analog Receiver Board - System Status-ADC Driver

- ADC Driver AD8131
  - Inputs a single-ended filtered signal
  - Output differential signal to the ADC
  - Used in RAPS design

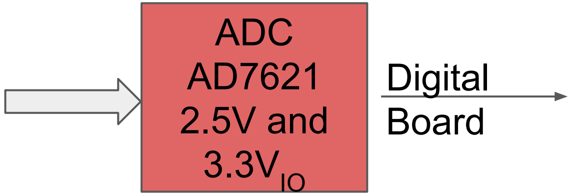


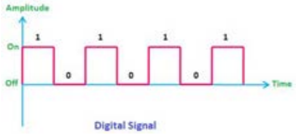


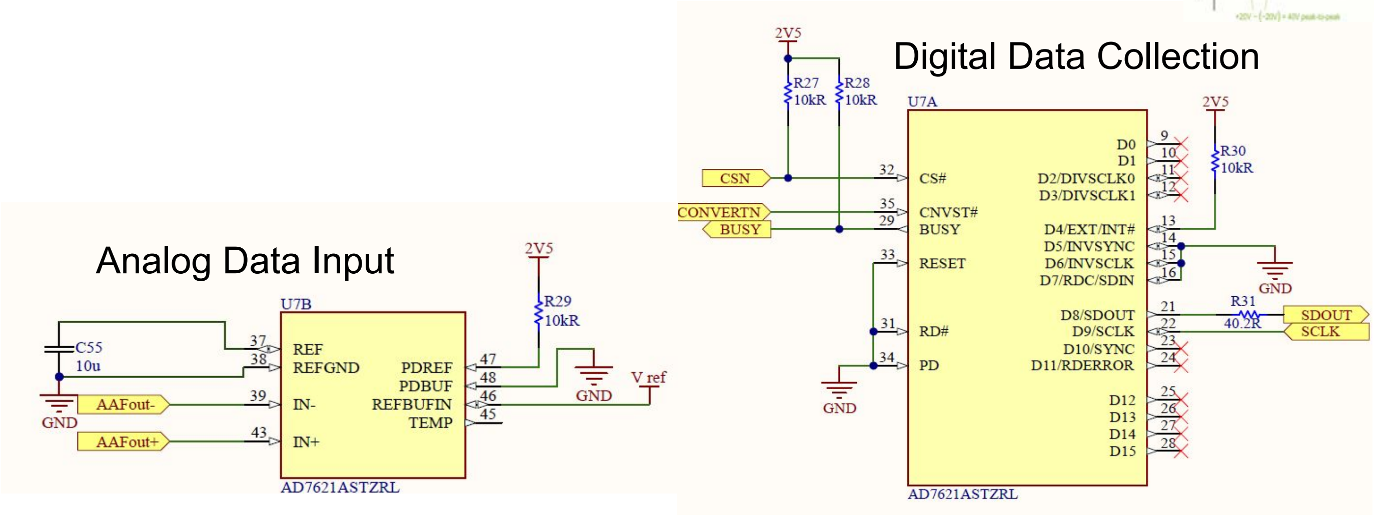


Analog Receiver Board - System Status-ADC

- ADC AD7621
  - 16-bit ADC
  - Based on RAPS design
  - Communicates with the digital board







Analog Receiver Board -Status-Layout

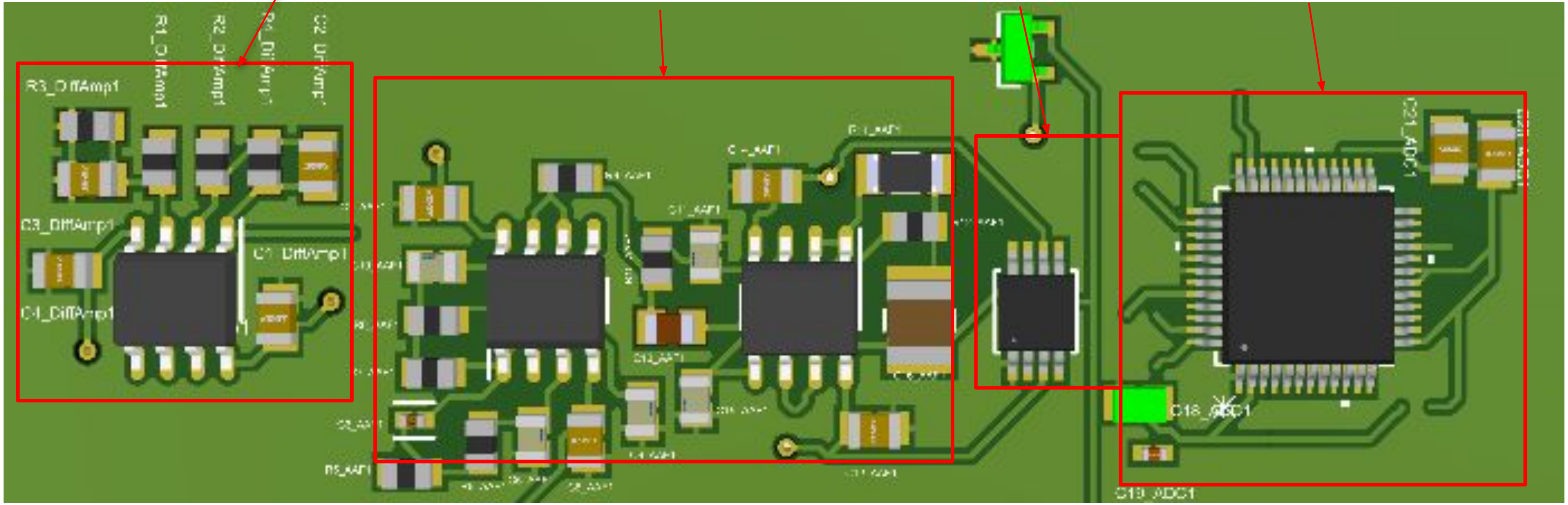
- Initial signal layout after Schematic Review

Differential Amplifier

Anti-Aliasing Filter

ADC Driver

ADC



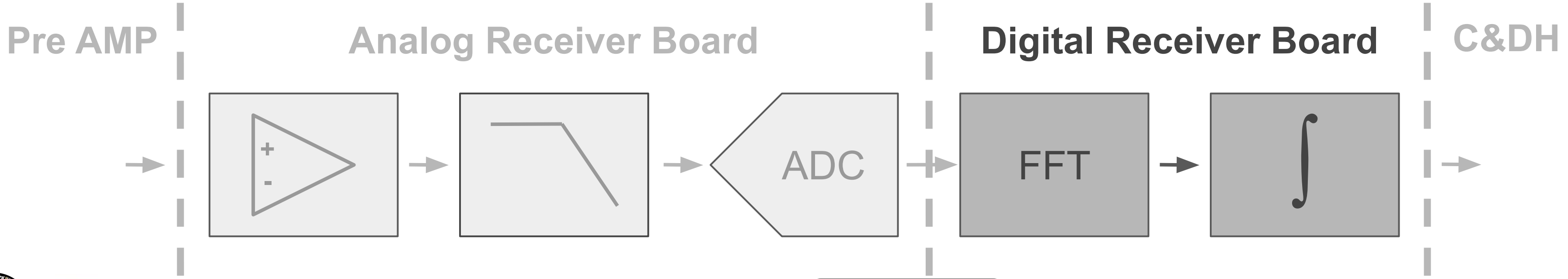
Analog Receiver Board - Next Steps

- Finish the layout and routing of the PCB in Altium.
  - Finalize the gain for the differential amplifier
    - Requires more in-depth research into literature on Whistler mode and DEMETER data.
  - Choose B-field preamp connector
  - Add clipping protection to the ADC.
  - Estimated: September 2020
- Order V1 of Analog board
- Test V1 for frequency response, sensitivity, and SFDR
- Detail mechanical interfaces to backplane and preamps
- Revisions for V2
  - Estimated: mid Fall 2020
- Full instrumentation subsystem integration and testing
  - Estimated: end of Fall semester 2020
- Detailed plans for Flight assembly boards
  - Estimated: Spring 2021

Digital Receiver Board - Overview

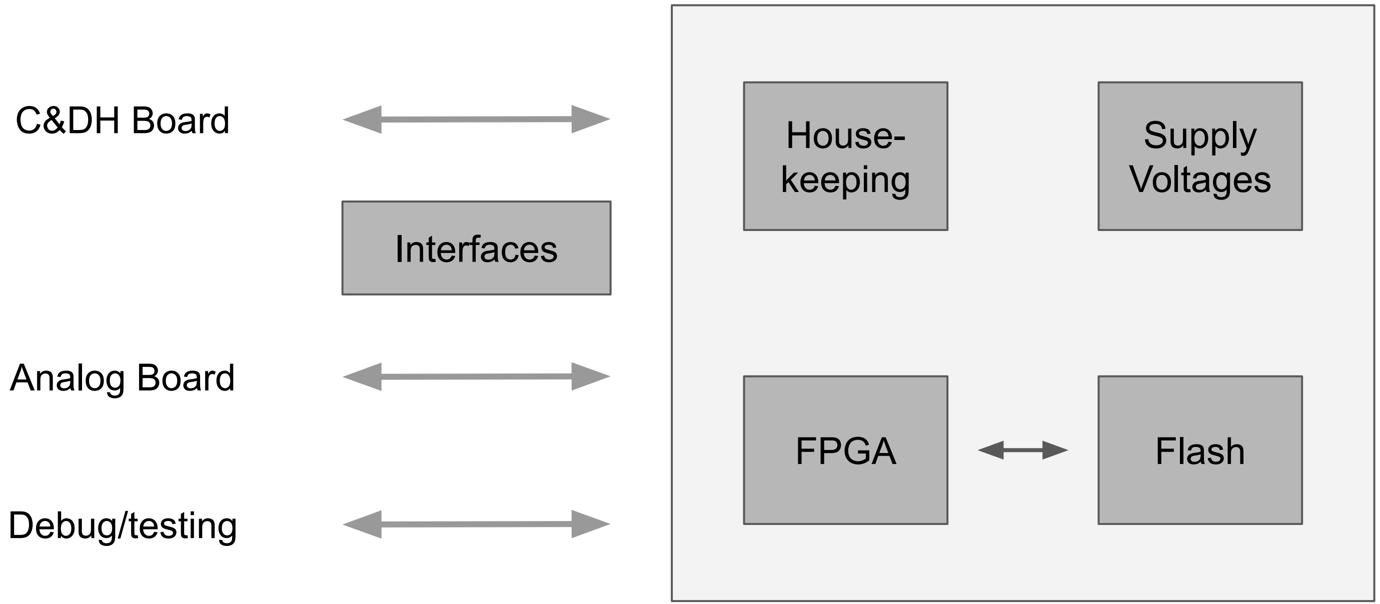
Main functionality

- Controls ADC conversion
  - 2^{17}Hz (131.072 kHz) Sampling Clk
  - SPI Master for digital data transfer
- Data processing and reduction
  - 1024 point FFT
  - Integration over 1 second
- Data transfer to C&DH



Digital Receiver Board - Overview

Functional overview

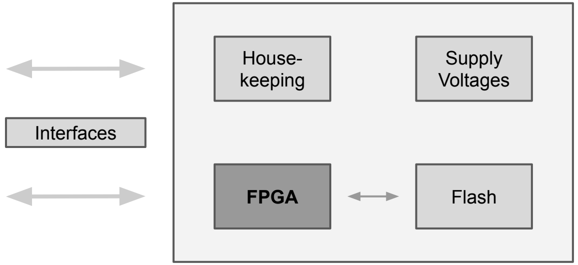


Digital Receiver Board - Key Requirements

Req.	Description	Reasoning
SCI-3	CANVAS shall be capable of providing user-defined data products.	Current data products being stored: Cross-Spectral matrix (17 bins for discrete transmitter frequencies, and remainder for the continuous frequency range)
SCI-4	CANVAS shall determine and report its position and attitude.	Required in order to know the ambient (terrestrial magnetic field) in the vicinity of the spacecraft, and for subsequent data processing.
SCI-4.3	CANVAS shall provide precise time-tagging of the data to within 0.5 seconds	CANVAS shall time-tag collected data for post-processing.

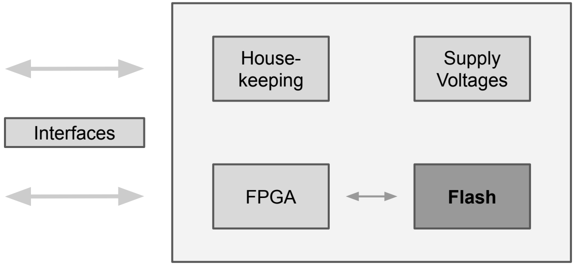
Digital Receiver Board - System Status

FPGA



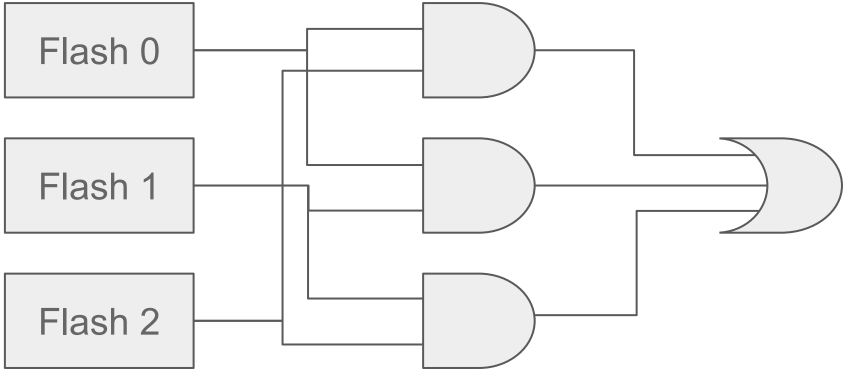
- Xilinx Kintex 7, 2^{24} Hz Clock
- Controls ADC conversion and data handling
- Processing and reduction of data
- Data transfer to C&DH board

Digital Receiver Board - System Status



Flash

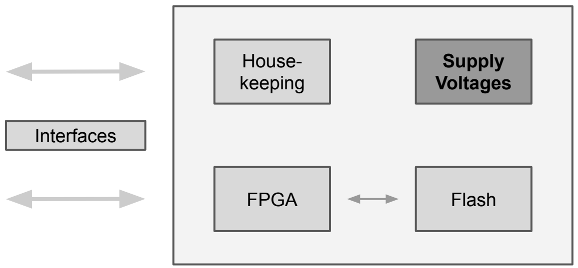
- Firmware for FPGA
- Error protection with majority function

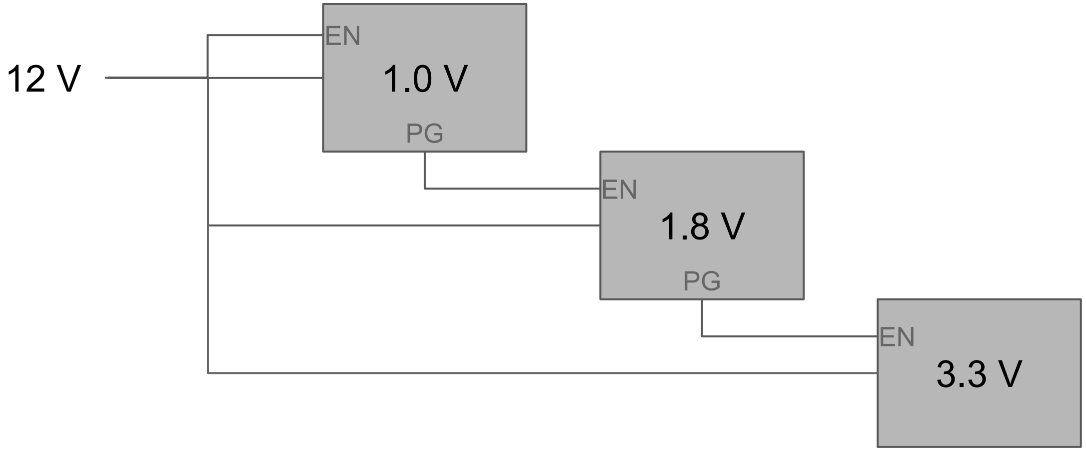


Digital Receiver Board - System Status

Supply voltages

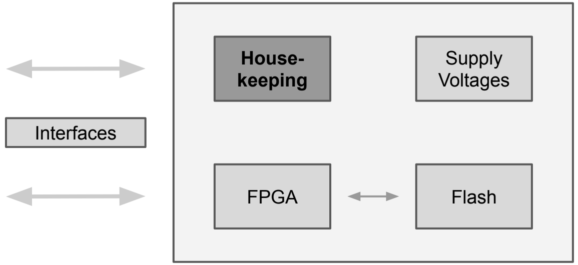
- Input: 12 V
  - Backplane or external connector
- Supply Voltages:
  - 1.0 V
  - 1.8 V
  - 3.3 V
- Output: 3.3 V
  - V_{IO} for ADCs on Analog Board





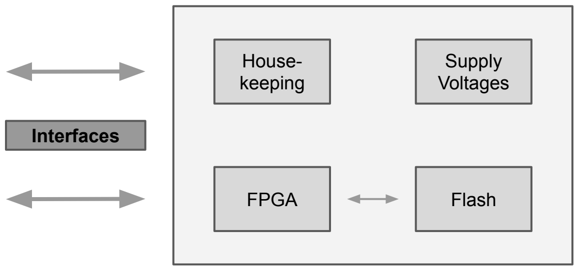
Digital Receiver Board - System Status

Housekeeping



- I2C-Slaves
- Temperature monitoring
- Voltage and current monitoring
- Overcurrent protection

Digital Receiver Board - System Status



Interfaces

- I2C (Housekeeping)
- RS422 (Control and data transfer to C&DH)
- Pulse per second (PPS)
- 5 x single slave architecture SPI buses (ADCs ARB)
- Control signals for ADCs on ARB
- JTAG
- LASP Testfixture
- Logic analyzer (tbd)

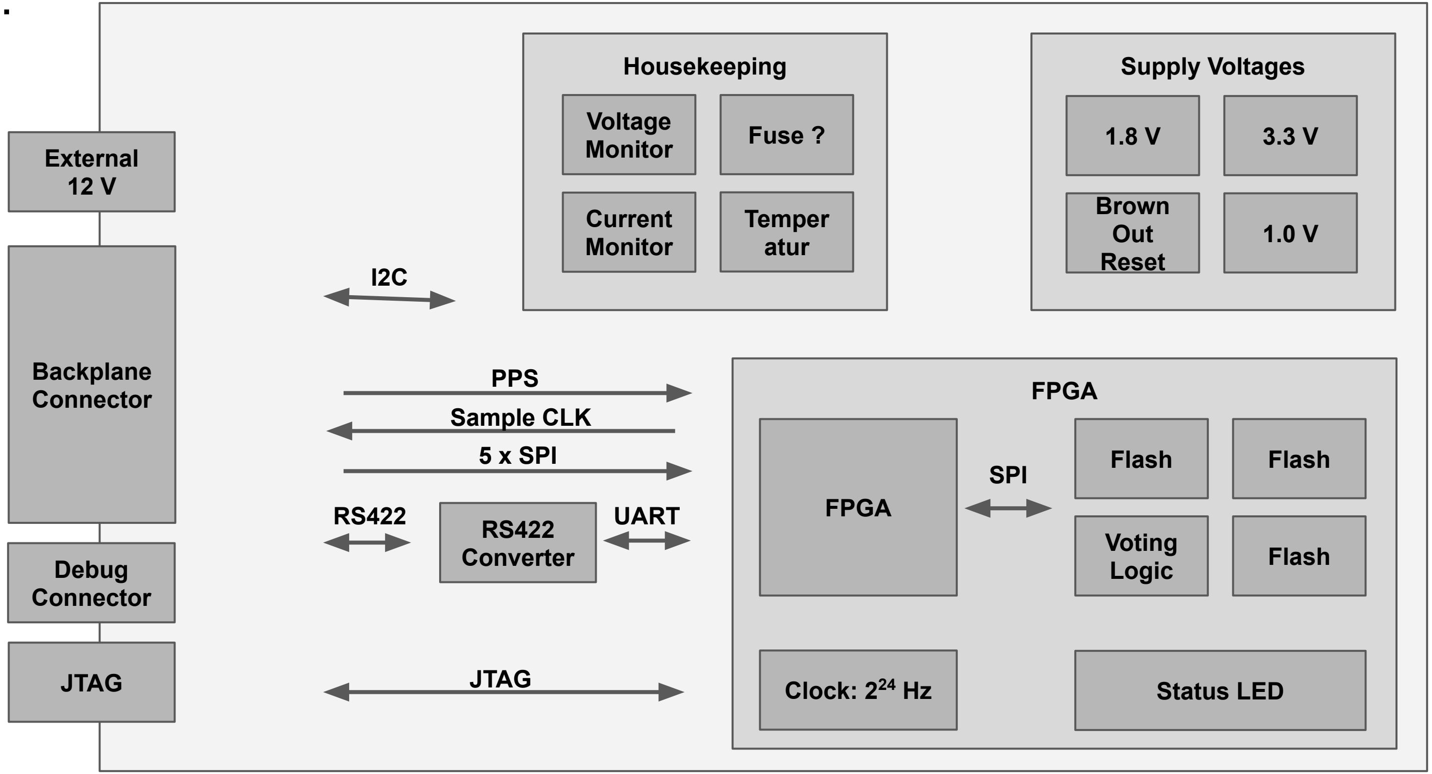
Digital Receiver Board - System Status

Features:

- Brown out reset
- Board decoupling filter
- Overcurrent protection (programmable fuse?)
- Current and temperature monitoring
- Placement variants for flexibility and testing
- Various debug and testing possibilities for firmware
- Power up sequence and delayed FPGA start to reduce inrush current

Digital Receiver Board - System Status

Block Diagram:



Digital Receiver Board - System Status

Status Update

- Schematic is about 90% finished
- Main components are defined and selected
- Connectors and signal assignment is determined
- FPGA pin assignment during layout process
- Adjust board to main reset concept
- I2C addresses tbd (flexible through placement variants)

Digital Receiver Board - Next Steps

Hardware

- Finishing schematic
- PCB development (Layout) 1st half of September
- PCB production and assembly
- Putting prototype into operation and testing end of September

Digital Receiver Board - System Status

Components: FPGA

Xilinx Kintex 7

- FBG676 Footprint
    - XC7K160T or XC7K325T
    - Extended temperature range (0°C - 100°C) or industrial temperature range (-40°C – 100°C)
- Clock
    - 2^{24} Hz (16.777216 MHz) oscillator, -20°C - 70°C
- Voltages
    - V_{INT}, V_{BRAM} 1.0 V
    - V_{AUX} 1.8 V
    - V_{IO} 3.3 V

Digital Receiver Board - System Status

Components: Voltage Converter

Linear Technology LT8610 Step-down Switching Regulator

- Radiation tested by CERN
- 12 V to V_{CC} conversion for maximum efficiency
- Lowest possible frequency for maximum efficiency (now 400 kHz)
- Frequency adjusted output ripple filter
- Enable cascade with power good signals

Digital Receiver Board - System Status

Components: Flash

Cypress S25FL128S 128 MBit NOR SPI Flash Memory

- V_{CC} and V_{IO}: 3.3 V
- 3 parts for error correction

Components: Differential Converter

Intersil ISL3180E High ESD Protected RS-485/RS-422 Transceiver

- 3.3 V for UART and RS422 bus

Digital Receiver Board - System Status

Components: Connectors

Backplane connector: Samtec QMS Series

- 8 power pins
- 52 (high speed) signal pins

JTAG: 2 x 7 pins, box header, male, 2 mm grid

External power jack: 12 V circular connector for single unit testing

LASP Testfixture: 2 x 7 pin, box header, male, 100 mil grid

Logic analyzer: tbd

Digital Receiver FPGA - Functional Description

- Data Sampling
    - Fetch digital samples from five ADCs concurrently
    - Sampling rate: 128KHz (i.e. 2^17Hz)
    - Perform rotational calculation on samples
- Perform Spectra calculation on each data source
    - Perform 1,024 point FFT with 50% overlap
    - Calculate the power for frequency bins 0 to 511
    - Accumulate power according to the binning specification
    - Integration period: 1 second
- Generate Spectra Telemetry Products for each data source
    - At a cadence of 1 second
        - Perform time and bin average on the accumulated Spectra power
        - Compress each power product
            - Perform SQRT on the 64-bit average value
            - Perform Pseudo-Log compression to generate 8-bit values

Digital Receiver FPGA - Functional Description

- Perform Cross-Spectra calculation on all permutations of Spectra
  - For each permutation
    - Fetch the Spectras power calculation terms
    - Calculate the Cross-Spectra power, real and imaginary, for frequency bins 0 to 511
    - Accumulate real and imaginary power according to the binning specification
    - Integration period: 1 second

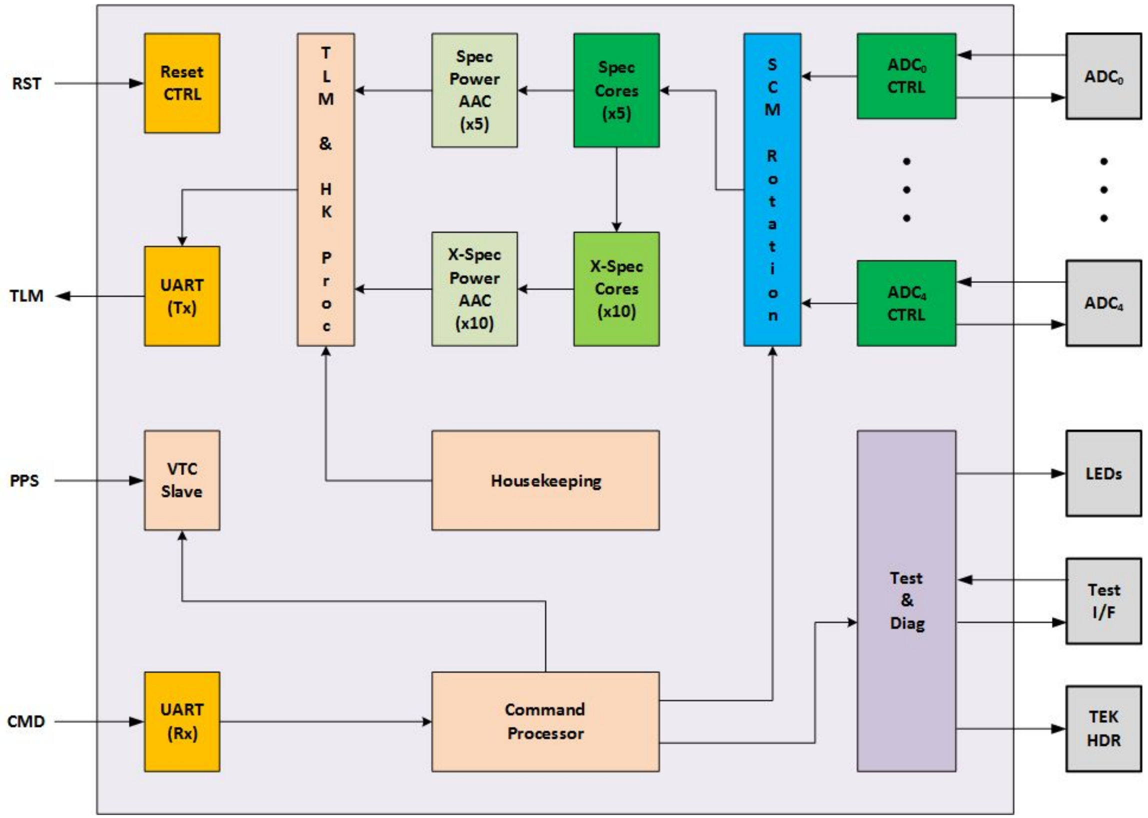
- Generate Cross-Spectra Products for each permutation
  - At a cadence of 1 second
    - Perform time and bin average on the real and imaginary accumulated Cross-Spectra power
    - Compress each power product
      - Perform SQRT on the 64-bit average value
      - Perform Pseudo-Log compression to generate 12-bit values

Digital Receiver FPGA - Functional Description

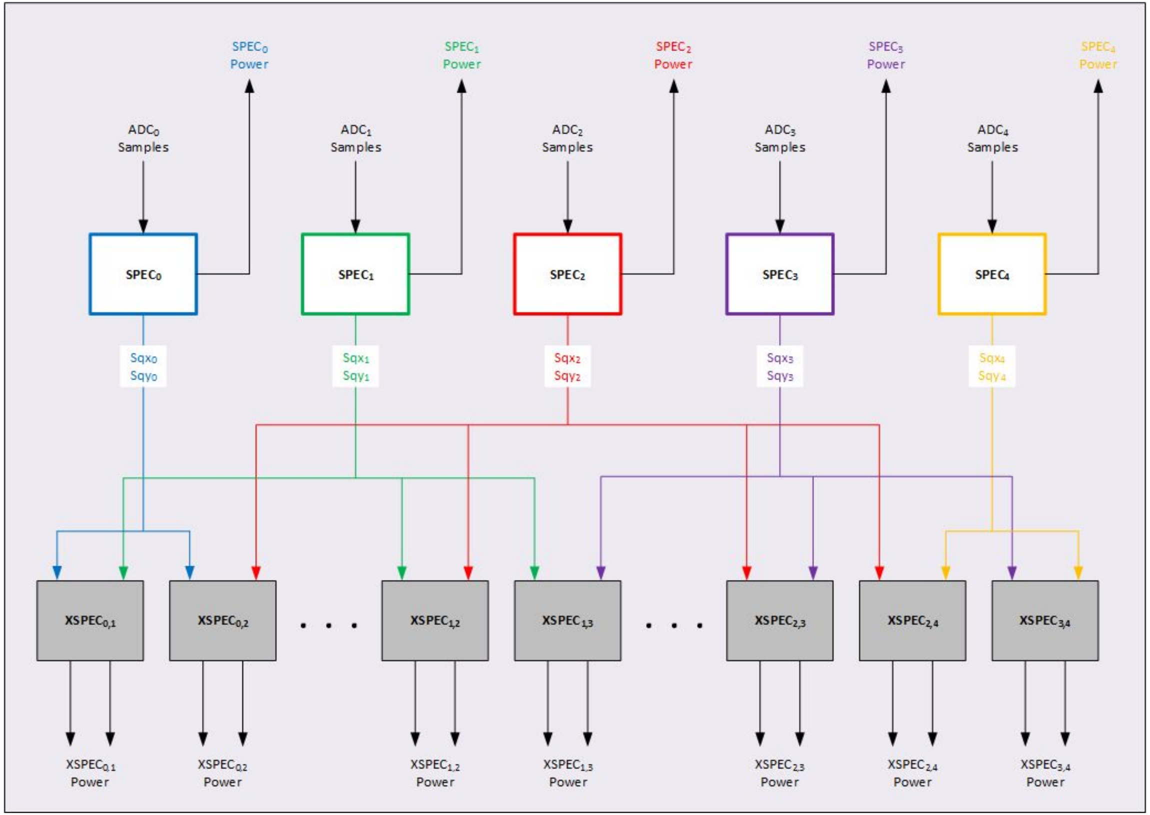
- Spectra & Cross-Spectra Telemetry
  - At a cadence of 1 second
    - Fetch Spectra & Cross-Spectra Products
    - Generate CCSDS packet
      - Timestamp packet with coarse and fine time
      - Packet's data field contains the Spectra/Cross-Spectra products
    - Transmit packet to C&DH using a UART
      - Baud rate: 115,200bps
      - Protocol: 8p1

- Commanding the FPGA
  - The C&DH can command the FPGA by
    - Using a UART, transmitting a CCSDS packet containing a command
      - Baud rate: 115,200bps
      - Protocol: 8p1

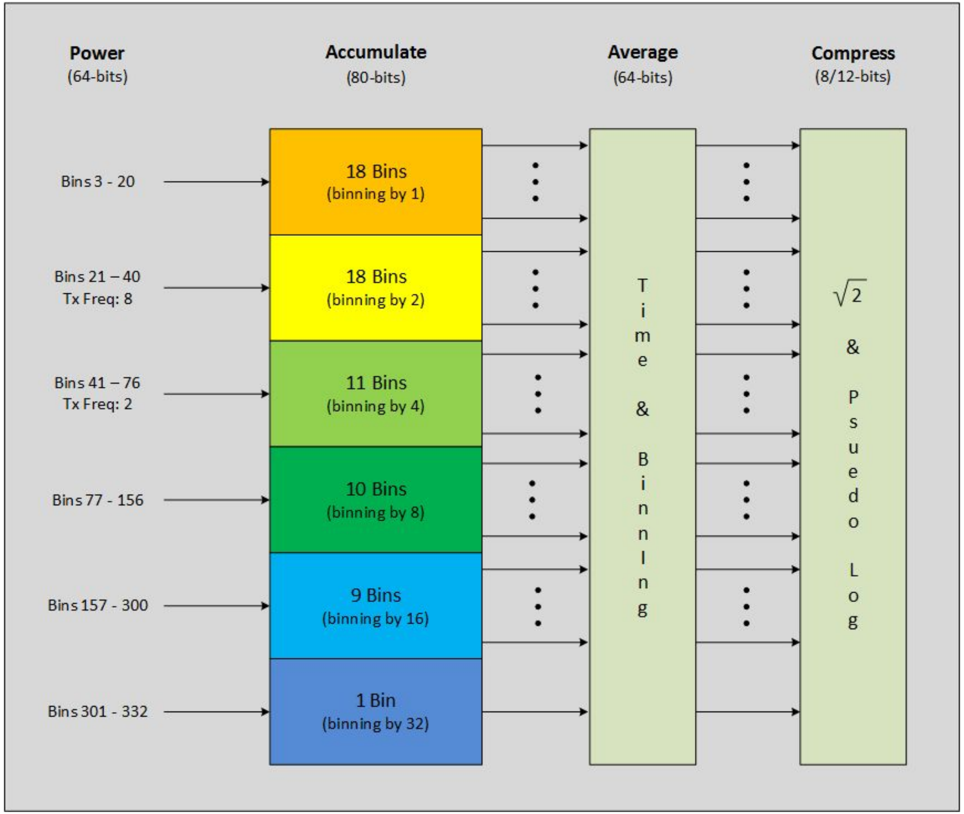
Digital Receiver FPGA - Block Diagram



Digital Receiver FPGA - X-Spec/Spec Cores



Digital Receiver FPGA - Accumulate/Avg/Compress



Digital Receiver FPGA - Status Update

- Micro-architecture for Spectra & Cross-Spectra is complete
- RTL code development is on-going

Digital Receiver FPGA - Next Steps

- Complete micro-architecture of CMD & TLM processors
- Creating Spectra/Cross-Spectra module level sim environment
- Provide Sebastian with bare-metal FPGA for use in the board bring-up
- Complete RTL code development

10 Minute Break

Return at 2:25pm

Structural Subsystem

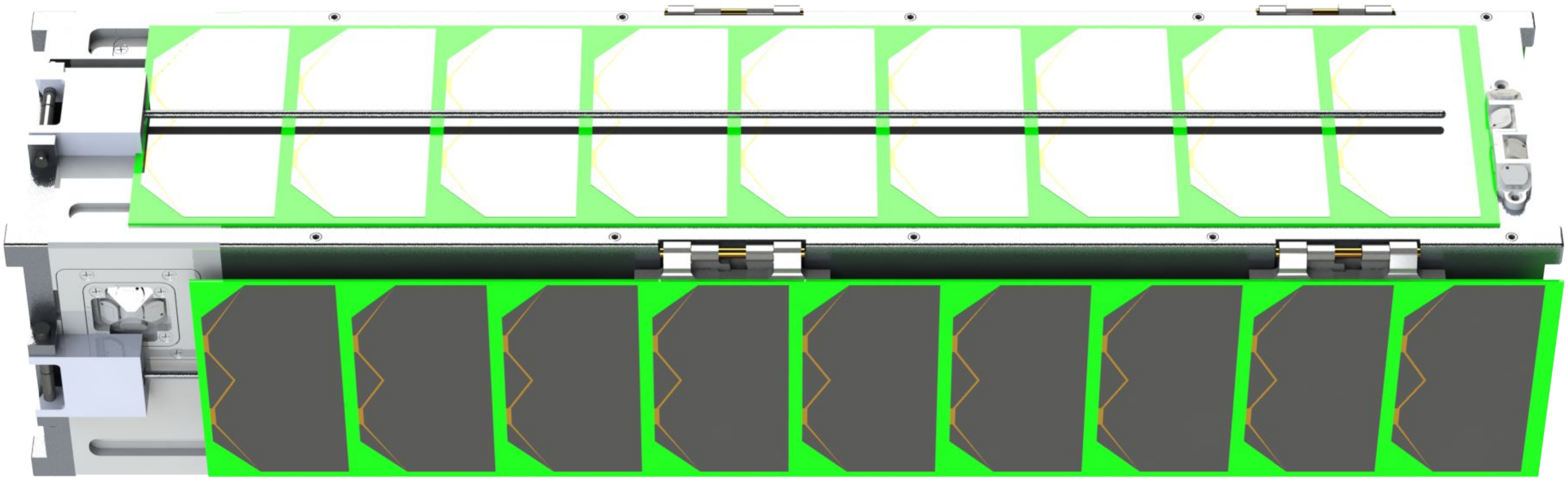
Dhruv / Kyle

CANVAS Presentation Schedule

Section	Presenter	Time	Duration
Introduction	Kyle	12:30 PM	0:05
S/C Overview and Mission Design	Kyle	12:35 PM	0:35
Instrumentation Intro	Riley	1:10 PM	0:05
E-Field Antennas	Kyle / Riley	1:15 PM	0:10
E-Field Pre-Amps	Keith	1:25 PM	0:10
B-Field Search Coils and Holder	Kyle / Riley	1:35 PM	0:05
B-Field Pre-Amps	Riley	1:40 PM	0:05
Analog Receiver Board	Riley / Keith	1:45 PM	0:10
Structures			
Bus Overview	Dhruv	1:55 PM	0:05
Fasteners and Analyses	Dhruv	2:00 PM	0:10
CTD Boom	Kyle	2:10 PM	0:05
Thermal	Shab	2:15 PM	0:10
Subsystems Part 1			
Power Budget, Solar Panels, Batteries	Ryan	2:25 PM	0:10
EPS	Jett	2:35 PM	0:15
10 Minute Break, return at 3:00pm			
Instrumentation Part 2			
Digital Receiver Board	Sebastian	3:00 PM	0:15
FPGA Development	Dr. Marshall	3:15 PM	0:10
Subsystems Part 2			
CDH	Chadd	3:25 PM	0:15
GSE	Max	3:40 PM	0:10
COMMs	Kyle	3:50 PM	0:05
S-Band / GPS Daughter Board	Jett	3:55 PM	0:05
Back Plane and Wiring	Dhruv / Jett	4:00 PM	0:10
ADCS / XACT	Kyle	4:10 PM	0:05
FSW	Lea	4:15 PM	0:05
Systems and Management			
Integration and Testing	Kyle	4:30 PM	0:05
Risk Analysis	Kyle	4:35 PM	0:10
Budget and Schedule	Kyle	4:45 PM	0:10
Questions and Feedback		4:55 PM	0:05
	End / Total	5:00 PM	4:30

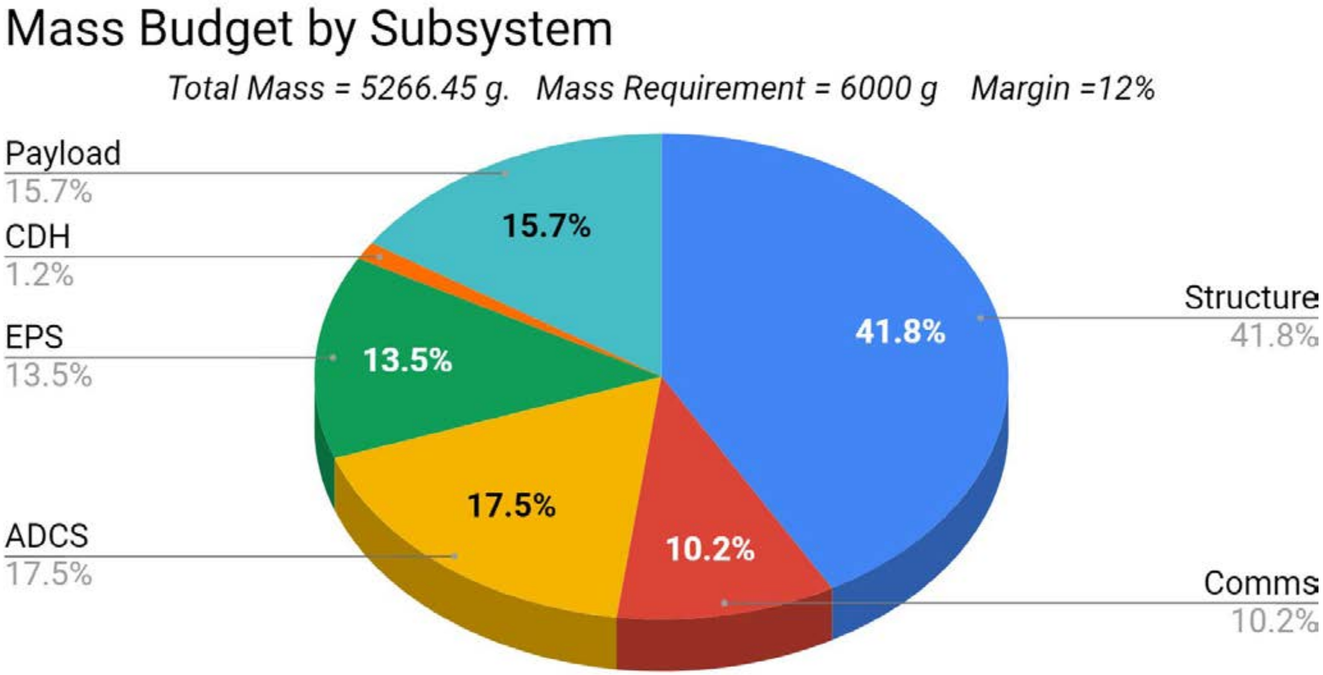
University of Colorado Boulder

Structures Overview



Structures subsystem is responsible for the overall mechanical design of CANVAS following the Nanoracks and the team requirements. Responsible for the overall structural integrity and integration of various components to successfully carry out the mission.

Bus Overview - Mass Budget



Mechanical Interfaces Overview

Lays out the list of the components CANVAS has followed by the interface each component has with the bus or other components in the assembly. The assembly matrix is a symmetric matrix that defines the interface in exactly one place in the lower triangle of the matrix. Each interface is labelled with the cell name which is referenced in the lists following the matrix i.e. Fasteners etc.

Finally, the Fasteners list entails all the structural interfaces present in CANVAS with the Screws/Bolt information from McMaster-Carr along with the number and type of the nuts and bolts required. It further refers to the Assembly Sequence Document

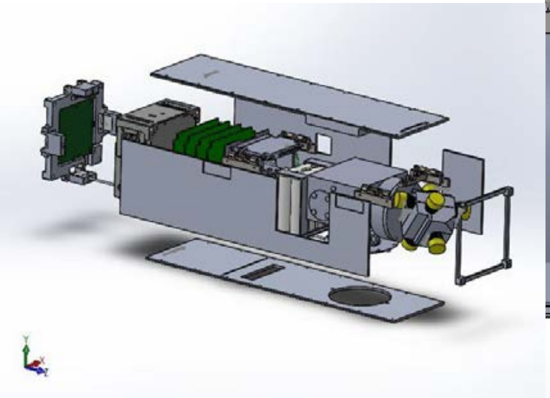
https://docs.google.com/spreadsheets/d/1KpNRD_qZ4jbCsV7A6cTpAT-RC0eTK5rjYIFaLcWO-0E/edit?pli=1#gid=1811889179

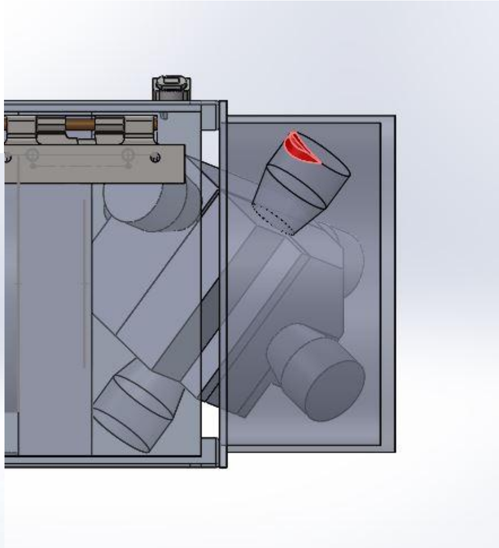
Structures - Key Requirements

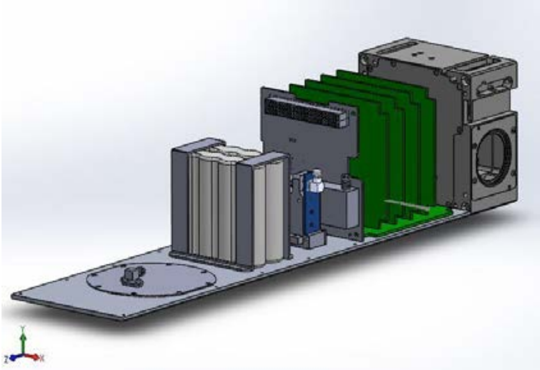
Req.	Description	Reasoning
STR-1	CANVAS shall conform to a 1x4U (4U) configuration	Must fit within Nanoracks specified 4U dimensions
STR-2	CANVAS shall not exceed 6.0 kg in mass	Must not exceed Nanoracks specified 4U mass
STR-13	The structure shall have a mechanical interface with CANVAS subsystems in accordance with subsystem ICD	Subsystem components must be anchored in satellite for safety and performance
STR-13.1	The subsystem shall provide mounting and harnessing for all other subsystems.	Subsystem components must be anchored in satellite for safety and performance

Bus Design - System Status

- Major design Challenges - Summer 2020
    - UHF Antenna - S - Band Antenna Orientations (Ideal - 90 deg)
    - Search Coil - Tuna Can Interference
    - Boom Mounting

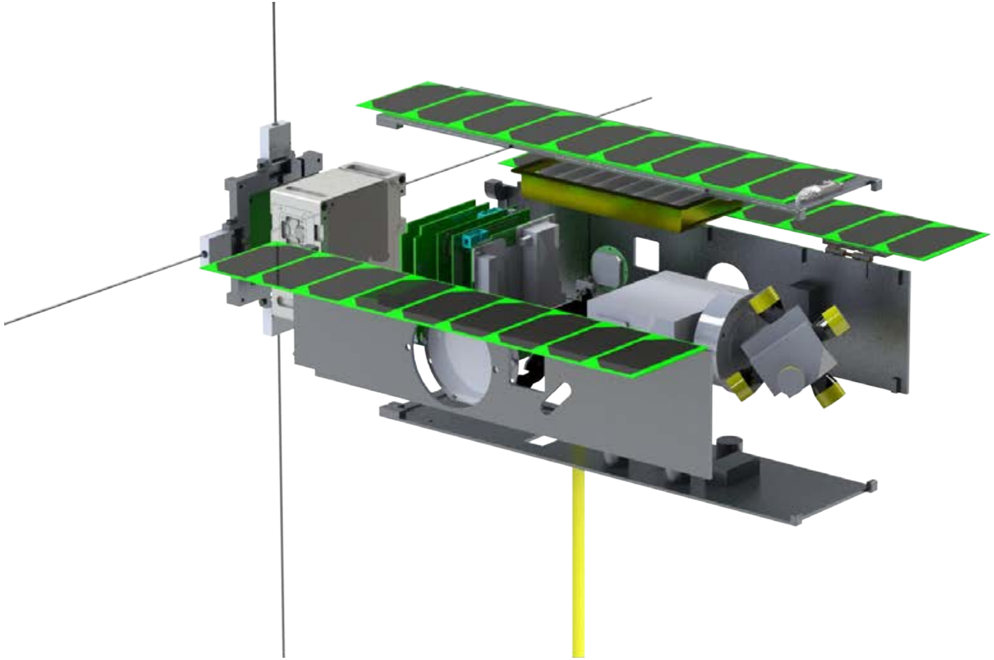




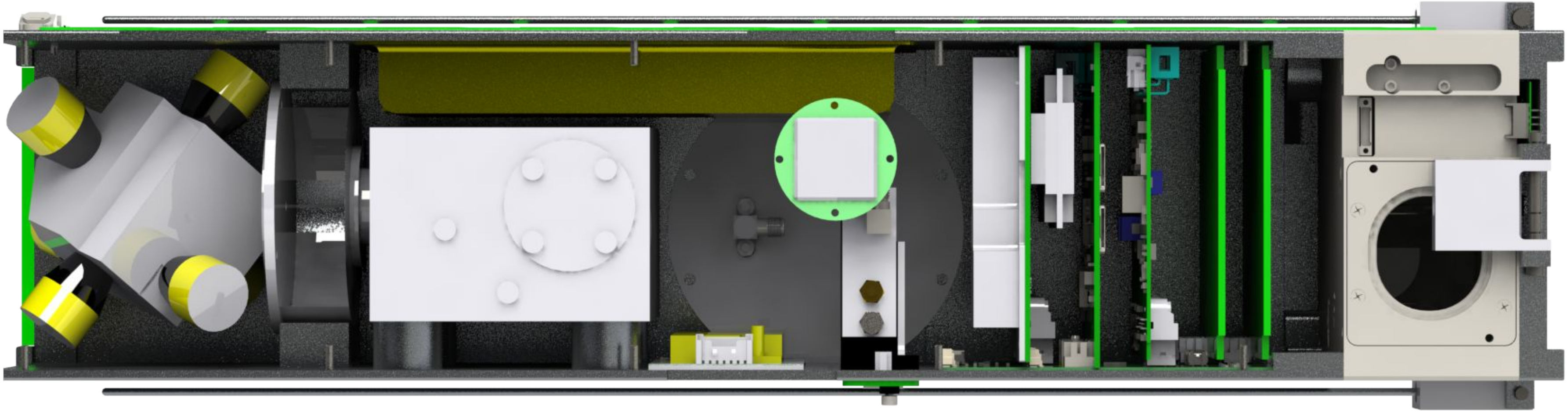


Panel Design

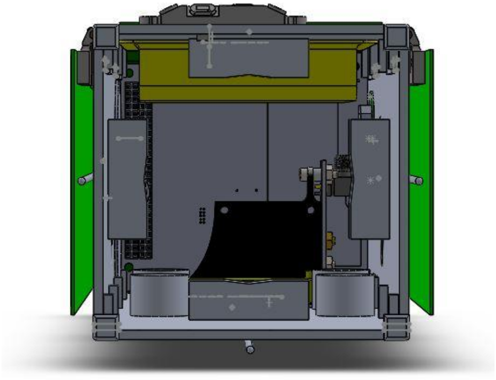
- ➔ 4U Cubesat (1 x 4)
- ➔ Five Panel Bus Design -
  - ◆ Top & Bottom Panel
  - ◆ Side Panels
  - ◆ XACT Crown
- ➔ Embedded Rail Ends
- ➔ Mounting Points - Extended mounts
- ➔ Panel thickness - 3mm
- ➔ Panel Material - Aluminium 6061 TS



Component Location



- ➔ Boom Mounting - Standoffs, Stabilizing Part, Slip Ring slots
- ➔ Battery Casing Mount
- ➔ S-Band Antenna



Mechanical Interfaces - System Status

Component List

COMPONENT LIST

Subsystem	Component	Sub-component
STR	Top Panel	
	Bottom Panel	
	Side Panel 1	
	Side Panel 2	
	XACT Crown	
	Battery Casing	
	Hinges(4)	Hinge Plates (8)
		Shaft (4)
		Springs (TBD)
		Washers (8)
	Guide Rails (8)	
	Nuts & Bolts	
	Stand-Offs	
	Switches (3)	
ADCS	XACT	
	Sun Sensors	
	Wires	
CDH	CDH Board	
	Backplane	
EPS	Batteries (2)	
	EPS Board	
	Solar Panels (3)	Solar Cells (27)
		(TBD)
		(TBD)
	Wires	

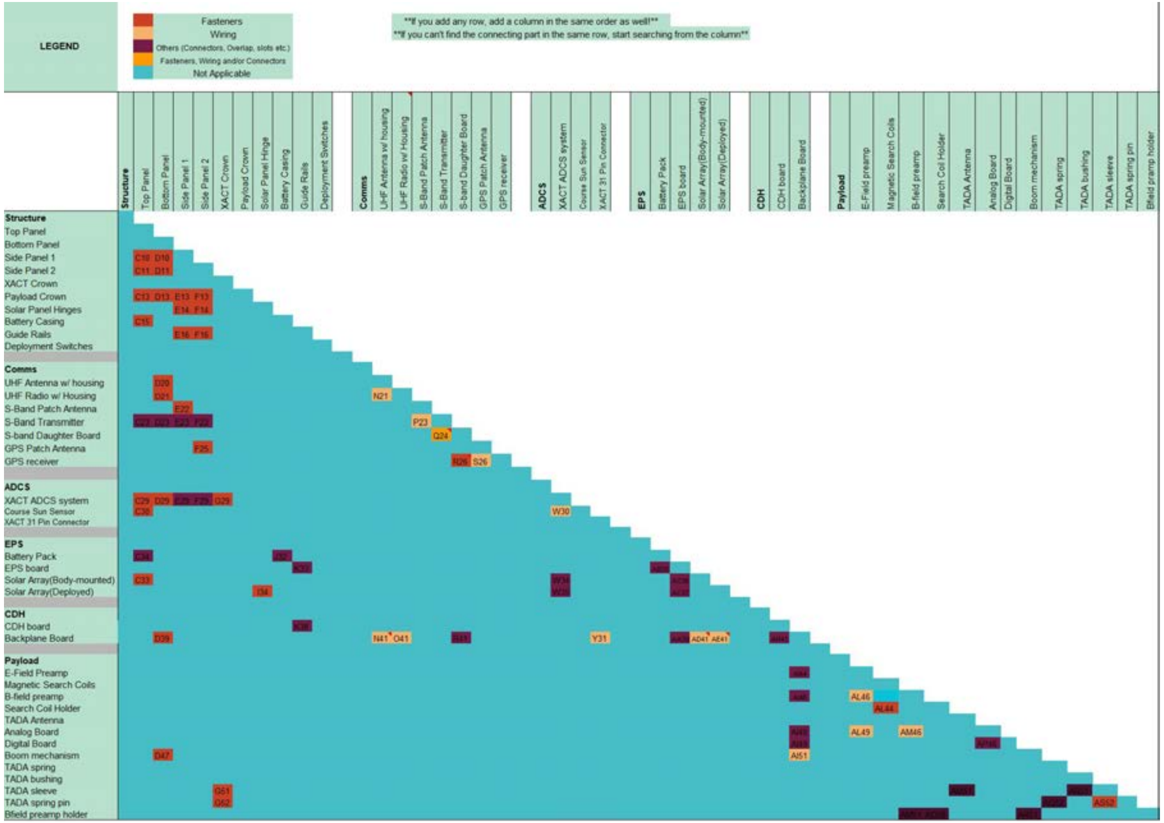
Subsystem	Group	Assembly	Component	Part
PL	E-Field	Antenna Housing(4)	Antennas (4)	
			Sleeve (4)	Box (4)
				Lid (4)
			Shaft (4)	
			Delrin (4)	
			Springs (TBD)	
			Washers (8)	
		E-Field Preamp		
		Analog Board		
		E-Field Wires		
	B-Field	Search Coils Housing	Search Coils (3)	
			Holder (3-piece)	
			B-field Preamp	
			B-field Preamp Holder	Box
				Lid
		Boom		
		Digital Board		
		B-Field Wires		
COMMS	S-Band Antena			
	Daughter Board			
	S-Band Receiver			
	GPS Patch			
	GPS Receiver			
	UHF Antenna Housing	House		
		Tape Antenna		
		Copper Pins		
		Hinge	Hinge Door	
			Hinge Pin	
			Hinge Springs	
		Nichrome Circuit Board		
	UHF Radio	UHF Radio Board		
	Wires			

Subsystem	Component
STH	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD
	TBD

- ➔ All components required for CANVAS Assembly
- ➔ Breakdown -
  - ◆ Subsystem
  - ◆ Subassembly
- ➔ Links to Fasteners, Washers and Wiring Spreadsheets

Master Assembly Matrix

- ➔ Demonstrates all Interfaces
- ➔ Divided into four categories
  - ◆ Fasteners
  - ◆ Wiring
  - ◆ Connectors, Overlaps, slots
  - ◆ Fasteners, Wiring &/or Connectors
- ➔ S-Band Transmitter - S-Band DB stands out (4th case)



Fastener Selection

- ➔ Interlinked with the Master Assembly
- ➔ Follows MINXSS heritage
- ➔ Uses Button Head Screws at most places instead of Flat Head Screws
  - ◆ Panel Dimensions
- ➔ Links to Mcmaster Carr for the exact screw dimension
- ➔ Interlinks with Assembly Sequence Document

Disclaimer - All Fasteners are based on the current part file available and the current CAD Design with the positions and dimensions of components like the Hinges and the panels

Fasteners

Master Assembly Matrix

Interface	Cell Number	Type of Fastener	Manufacturer	Number of Fasteners	Type of Nuts (If any)	Type of Holes	Assembly Sequence Number
Side Panel 1 - Top Panel	C10	18-8 Stainless Steel Socket Head Screw, 2-56 Thread Size, 3/8" Long	McMaster-Carr	5	-	Top Drill/Tap Hole	X
Side Panel 1 - Bottom Panel	D10			5	-	Top Drill/Tap Hole	X
Side Panel 2 - Top Panel	C11			5	-	Top Drill/Tap Hole	X
Side Panel 2 - Bottom Panel	D11			5	-	Top Drill/Tap Hole	X
Payload Crown - Top Panel	C13	Black-Oxide Alloy Steel Socket Head Screw, 5-40 Thread Size, 3" Long	McMaster-Carr	1	-	Top Drill/Tap Hole	X
Payload Crown - Bottom Panel	D13			1	-	Top Drill/Tap Hole	X
Payload Crown - Side Panel 1	E13			1	-	Top Drill/Tap Hole	X
Payload Crown - Side Panel 2	F13			1	-	Top Drill/Tap Hole	X
Solar Panel Hinges - Side Panel 1	E14	TBD	McMaster-Carr	2	Hex Nut	Drill Hole	X
Solar Panel Hinges - Side Panel 2	F14			2		Drill Hole	X
Battery Casing - Top Panel	D15	18-8 Stainless Steel Phillips Flat Head Screw, Passivated, 4-40 Thread Size, 1/2" Long	McMaster-Carr	10	Hex Nut	Drill Hole	X
Guide Rails - Side Panel 1	E16	18-8 Stainless Steel Button Head Hex Drive Screw, 4-40 Thread Size, 3/8" Long	McMaster-Carr	8	In Built - Swage Nut	Drill Hole	X
Guide Rails - Side Panel 2	F16			8		Drill Hole	X
UHF Antenna Housing - Bottom Panel	D20	18-8 Stainless Steel Button Head Hex Drive Screw, 4-40 Thread Size, 3/8" Long	McMaster-Carr	6	Hex Nut	Drill Hole	X
UHF Radio Housing - Bottom Panel*	D21	18-8 Stainless Steel Button Head Hex Drive Screw, 4-40 Thread Size, 3/8" Long	McMaster-Carr	4	Press-Fit Nut	Drill Hole	X
S-Band Antenna - Side Panel 1	E22	18-8 Stainless Steel Socket Head Screw, 8-32 Thread Size, 3/8" Long	McMaster-Carr	4	Hex Nut	Drill Hole	X
S-Band Antenna - S-Band DB	Q24	18-8 Stainless Steel Socket Head Screw, 8-32 Thread Size, 5/16" Long		4	Press-Fit Nut	Drill Hole	
GPS Patch - Side Panel 2	F25	18-8 Stainless Steel Socket Head Screw, 4-40 Thread Size, 3/8" Long	McMaster-Carr	4	Press-Fit Nut	Drill Hole	X
GPS Reciever - S-Band DB	R26	18-8 Stainless Steel Socket Head Screw, 8-32 Thread Size, 9/16" Long	McMaster-Carr	4	Lock Nut	Drill Hole	X
XACT System - Bottom Panel	D29	Black-Oxide Alloy Steel Socket Head Screw, 5-40 Thread Size, 3" Long	McMaster-Carr	1	-	Tap Hole, Dowel Hole	X
XACT System - Side Panel 1	E29			1		Tap Hole, Dowel Hole	X
XACT System - Side Panel 2	F29			1		Tap Hole, Dowel Hole	X
XACT System - XACT Crown	G29			1		Tap Hole, Dowel Hole	X
Solar Panel (Body Mounted) - Top Panel	C33	18-8 Stainless Steel Button Head Hex Drive Screw 4-40 Thread Size, 3/8" Long	McMaster-Carr	4	Press-Fit Nut	Drill Hole	X
Solar Panel (Deployed) - Hinges	I34	TBD	McMaster-Carr	8	Lock Nut	Drill Hole	X
Backplane - Bottom Panel	D39	18-8 Stainless Steel Socket Head Screw, 4-40 Thread Size, 3/8" Long	McMaster-Carr	5	Press-Fit Nut	Drill Hole	
Boom Mechanism - Bottom Panel	C47		McMaster-Carr	4	-	Drill Hole	X

Structures - Next Steps

- 3 Standard Analyses - Stress-Displacement, Natural Frequency and Random Vibe
  - Validate mechanical design choices made to adhere NRCSD Requirements
  - Models ready - Just need to update the model with the updated CAD to run the simulations
- **Hinge Design**
  - Rails are currently discontinuous and doesn't obey the NRCSD Requirement.
  - The design has to keep in mind the deployment sequence decided over the Summer i.e. Solar Panels -> E-Field Antenna
- Deployment Mechanisms
  - Potential concerns with Solar Panels and E-Field Deployments
- Wiring
  - Use SolidWorks Routing toolbox to model the big wires to check for bend radii and routing plan Eg. S-Band Antenna - Transmitter Card, UHF Antenna - Radio Housing
- Assembly Sequence Document
  - Detailed plan and layout of all the component integrations and assembly with elaborative pictures to facilitate the process

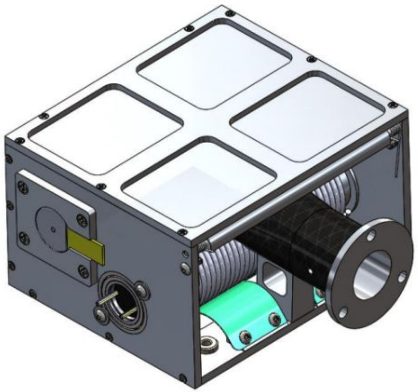
CTD Boom - Overview

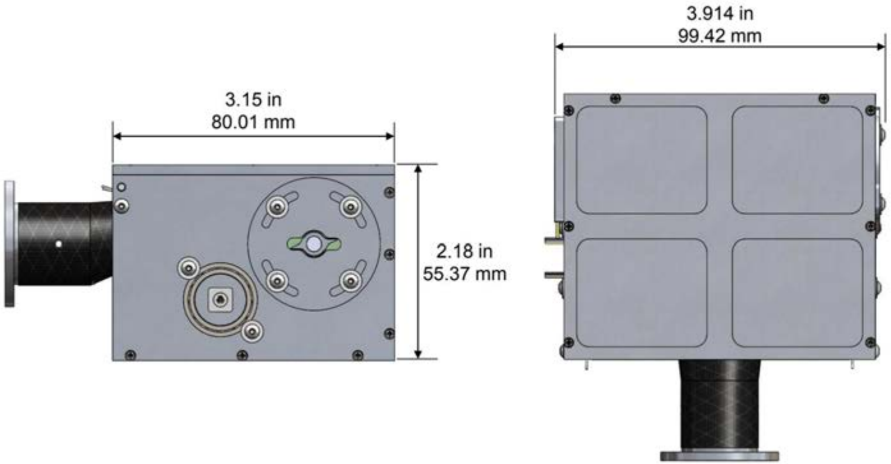
Images sourced from CTD Requirements and Overview Submittal

- *Deployed Length*: 1 meter
- *Diameter*: 21.84mm +/- 1mm
- *Mass*: 480 grams
- *Power*: 12V, deployment only

The CTD boom will carry the Magnetic Search Coil Holder away from the spacecraft to magnetically isolate the sensors.

Signals and power are sent through 4 shield, twisted pairs and a COTS slipring.





CTD Boom - Key Requirements

Req.	Description	Reasoning
STR-13.1	The structures subsystem shall provide mounting and harnessing for all other subsystems	The structure has to be able to incorporate the CTD boom housing.
SCI-2.2	CANVAS shall measure electric fields with sensitivity less than 10^-4 nT/rt-Hz in the band of interest	Observed whistler wave amplitudes from previous missions impose reqs. for sensitivity. The search coils shall be 1 [m] away from the bus to meet this requirement. The vicinity of the search coils shall also be devoid of metallic elements

CTD Boom - Requirements for CTD

Requirement Title	Statement	Min	Max	Units	Verif. Method
Physical Requirements					
Total Mass	The boom and deployer system shall weigh no greater than 0.5 kg	-	0.5	*kg*	Measure
Boom Diameter	The boom system shall have a deployed diameter between 0.7" and 1.25"	0.7	1.25	*in*	Measure
Boom Deployed Length	The boom shall have a fully deployed length of 1 meter	1	1	*m*	Measure
Payload Mass	The boom shall incorporate a tip payload mass of 500 grams	-	500	*grams*	
Payload Signal Cables	The boom/deployer shall enable 3 shielded, twisted pair cables for signals between the spacecraft (boom root) and instrument payload (boom tip)	-	3	*shielded, twisted pair*	Design/Acceptance
Payload power wiring	The boom/deployer shall enable a single shielded, twisted pair (Gore DXN2605) for power between the spacecraft (boom root) and instrument payload (boom tip)	-	1	*shielded, twisted pair*	Design/Acceptance
Payload Wiring	Deployer must use Gore shielded wiring with part number DXN2605	-	-	-	Design/Acceptance
Slip Ring [Signal and Power]	At the boom root, signal cables will be routed through an un-shielded COTS slip-ring. The deployer must use Orbex Group slip ring with part number 312M3-1200	-	-	-	Design/Acceptance
Deployed Resonant Frequency	The boom and payload system shall have a deployed resonant frequency of 0.5 Hz or higher	0.5	-	*Hz*	Analysis
Stowed Volume	The boom system shall occupy no greater than 0.5U when stowed	-	0.5	*U*	Design/Measure
Launch Restraint	The boom system shall incorporate a resettable launch-restraint feature	-	-	-	Design/Acceptance Test
Deployment Confirmation	The boom system shall provide a measurable indication of deployed distance via rotary encoder or other device	-	-	-	Design/Acceptance Test
Performance Requirements					
Boom/Payload Position Characterization	The boom and payload shall be characterized to determine position in fully-deployed "0G" condition	-	-	-	Test
Boom Tip Deflection (Distal End)	The boom shall not deflect more than 1 cm at the distal end (due to thermal distortion or other loading)	-	1	*cm*	Analysis
Boom Twist Angle	The boom must utilize slit-lock and meet the required twist of less than 1 degree	-	1	*deg*	Design/Acceptance Test
Deployment Voltage	The boom system shall deploy the sensor using no greater than 12V.	-	12	*V*	Acceptance Testing
Deployment Power	Deployment power shall not exceed 2W	-	2	*W*	Acceptance Testing
Deployment Time	Deployment time shall not exceed 8 minutes per axis	-	8	*Min*	Acceptance Testing
Environmental Requirements					
Random Vibration	The boom system shall be capable of surviving a 14.1 grms random vibration environment as specified by NASA-GEVS	14.1	-	*grms*	Vibration testing
Deployment Temperature	The boom system shall be capable of deploying within a temperature range of -25°C to 40°C	-25	+40	*C*	Thermal Deployment Acceptance Testing
Interface Requirements					
Mechanical ICD	The boom system shall conform with a released Mechanical ICD document	-	-	-	Documentation
Electrical ICD	The boom system shall conform with a released Electrical ICD document	-	-	-	Documentation

Key Takeaways:

CTD required to meet:

- Deployed resonant frequency>.5 Hz with 500 gram tip mass
- Deployed by 12V power
- Incorporate a slipring
- Adhere to NASA-GEVS random vibe
- Operate in -25-40 C
- 1 meter boom
- <.5 kg mass

CTD Boom - Status

Analysis completed for a similar design:

- 1.3 m long
- 0.8” diameter
- 638 g payload mass

Current design will have a higher frequency

- Not as long
- Wider diameter
- Nearly ½ the payload mass

Pre-Load (lbsf)	1st Natural Frequency (Hz)	Maximum Principal Stress (compression) (psi)
0.5	0.75	24.6
1.0	0.87	49.2
1.5	0.92	73.9
3.0	0.93	148.0

CTD Boom - Next Steps

- CTD Boom - B-Field Payload Interface Definition
  - The Boom plate connection with the B-Field Preamp holder followed by the B-field Preamp Holder and Search Coil Holder Connection
- Deployment testing
  - CTD's Acceptance testing includes:
    - A minimum of 3 full stow and deployment cycles in a lab environment at room temp.
    - Perform thermal deployment testing in a thermal chamber (@-25C and +40C)
      - Will only include first 6 inches of boom
  - CTD advises against user deployment tests due to complicated deployment reset procedure - this is an added and documented risk
- Delivery date likely early September

Thermal Subsystem

Shab

Thermal - Key Requirements

Req.	Description	Reasoning
TCS-1	The subsystem shall maintain all components within operational temperature limits during Normal Operations Mode	Due to the temperature fluctuations in space we want to assure none of the spacecraft components get too cold and leave their temperature limits.
TCS-2	The subsystem shall maintain all components within survivable temperature limits for mission duration	Due to the temperature fluctuations in space we want to assure none of the spacecraft components get too cold and leave their temperature limits.

Thermal - Overview

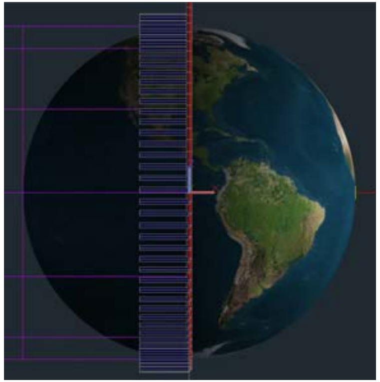
- Temperature Sensors will be used to monitor the temperatures for all critical subsystem components
- Heaters will be used to keep batteries above minimum operating temperature
- Thermal coatings and conduction will be used to keep components from overheating
- Aluminum panels will be used as heat sinks/radiative surfaces
- Minimize conduction from solar panels to chassis

Thermal - Operating Temperature Requirements

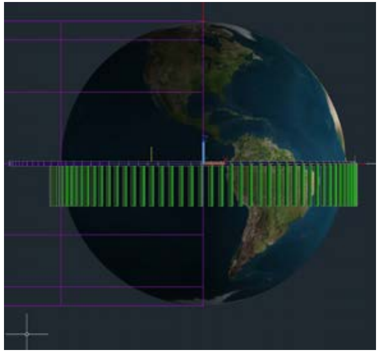
Subsystem	Component	Operating Temp
ADCS	XACT	-20 to 60
	GPS	-45 to 85
EPS	Batteries	0 to 40
	EPS Board	-30 to 70
	Solarpanels	-75 to 100
	Body Mount SP	-75 to 100
COMMs	Sband Radio	-25 to 61
	UHF Radio	-30 to 70
CDH	CDH Board	-25 to 85
	Backplane	-30 to 70
PAYLOAD	analog board**	-30 to 70
	digital board**	-30 to 70
	E preamp**	-30 to 70
	Bpreamp**	-30 to 70

** operating temperature are unknown, current values reflect CDH/EPS board

Orbital Analysis Scenarios



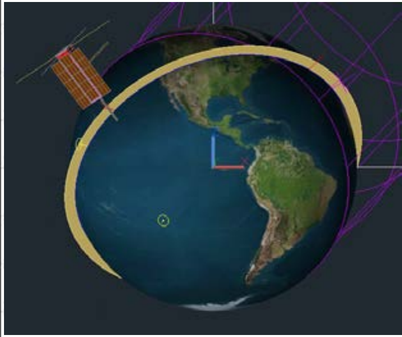
WCH



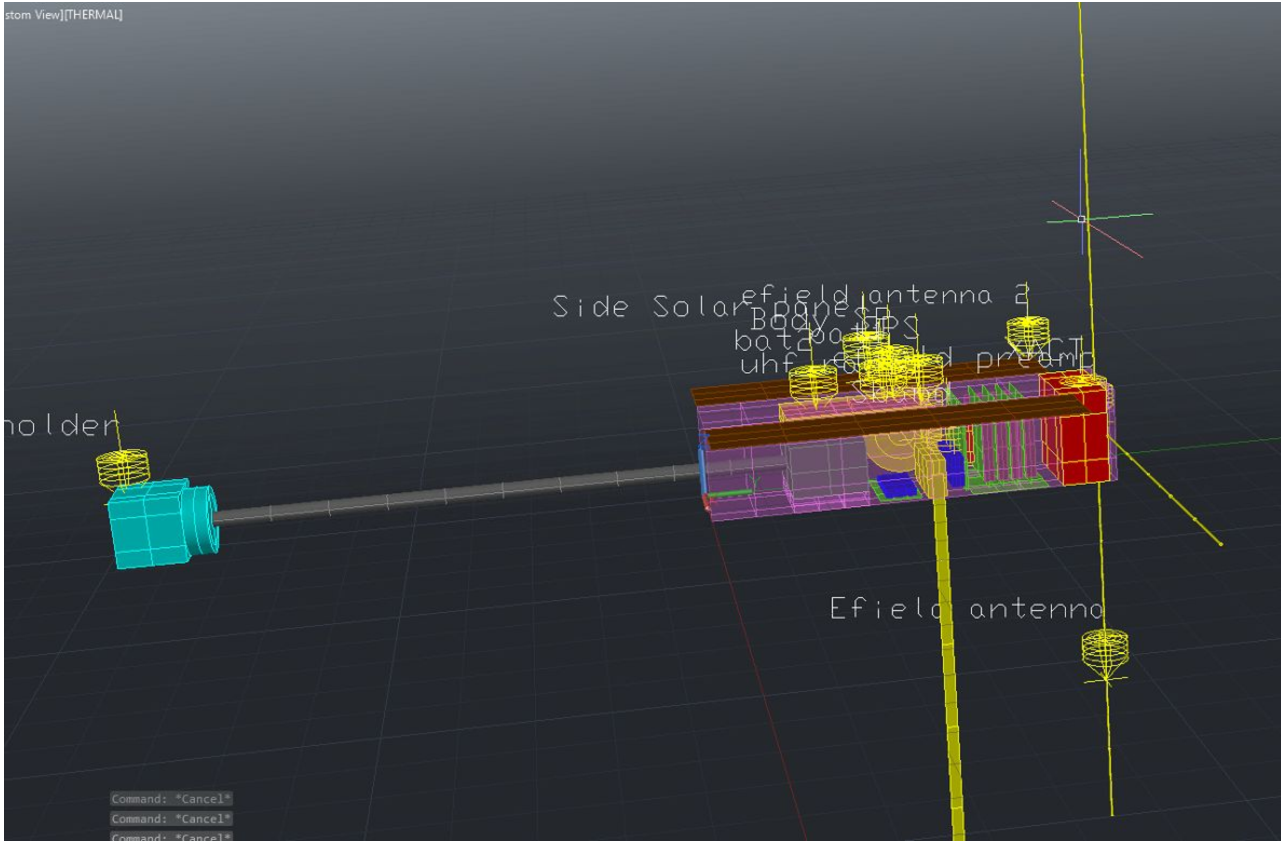
WCC

0	Worst Cold	Worst Hot	Reference Kepler Orbit
Altitude, km	500	500	500
Inclination	0	90	51.6
β Angle	0	90	-49
Ref. Date for RA	N/A		12/01/2021
RAAN	0		202
Albedo	0.35		
Eccentricity	0		
Period	5677		
Radios	Off	On(16mins/day)	On(16mins/day))
Battery	No discharge/charge	0.35W	
ADCS	On(1.35W)	On(2.82W)	On(1.92W)
CDH	0.91W		
EPS	0.1W		
EField Preamp	Off	0.27W	
Analog Board	Off	2W	

Actual

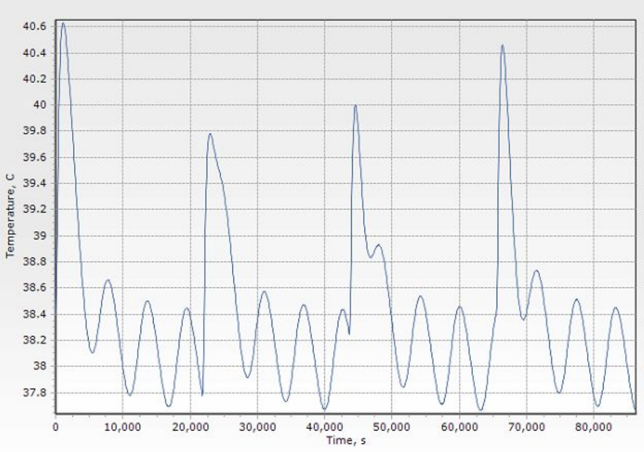


Thermal Desktop Model

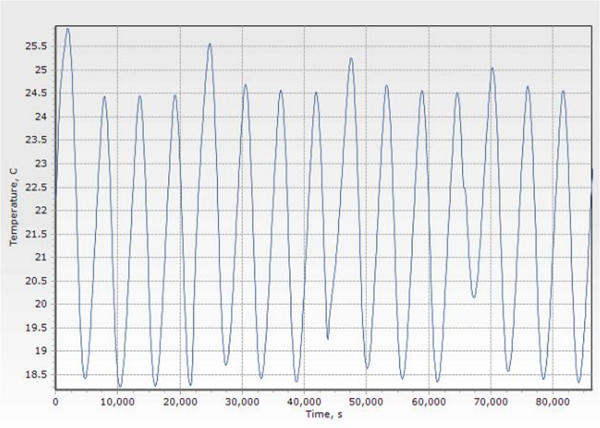


Results - Sband Radio

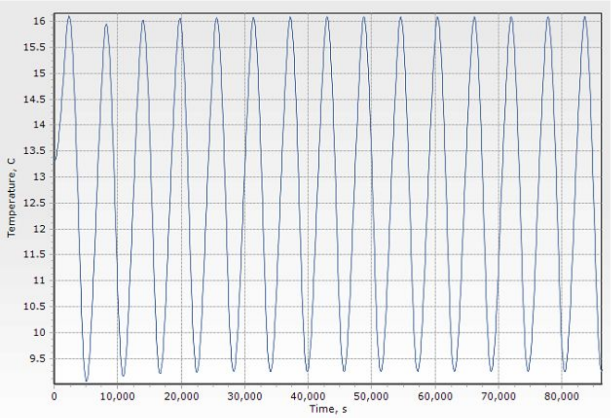
Worst Case Hot



Actual Case



Worst Case Cold

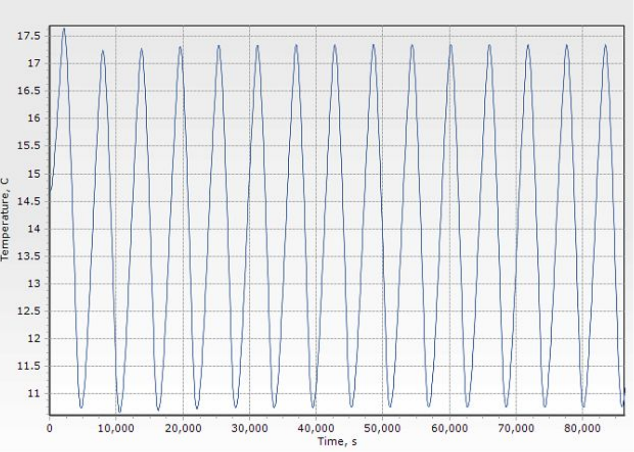


Results

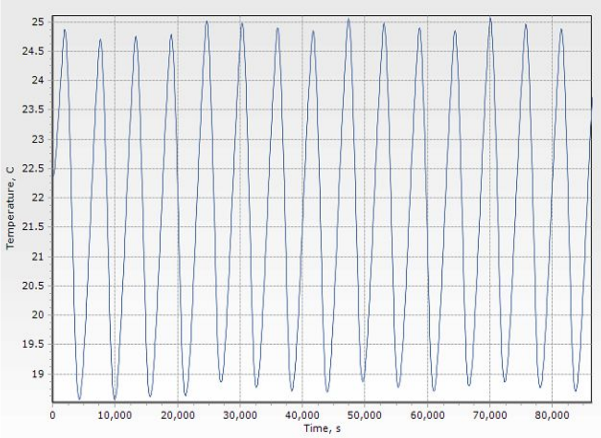
Component	Worst Case Cold	Actual Ref. Case	Worst Case Hot
Batteries	0 40 11 17	0 40 19 25	0 40 37 39
CDH	-25 85 6 14	-25 85 42 49	-25 85 60 63
EPS	-30 70 6 16	-30 70 25 33	-30 70 45 47
Efield Preamp	-30 70 2 14	-30 70 12 22	-30 70 35 36
Sband Board	-25 61 9 16	-25 61 18 26	-25 61 37 41
Solar Panels	-75 100 -50 80	-75 100 -45 80	-75 100 77 82
UHF Board	-30 70 2 15	-30 70 11 24	-30 70 34 37
XACT	-20 60 2 14	-20 60 11 22	-20 60 34 36

Battery Heater Analysis

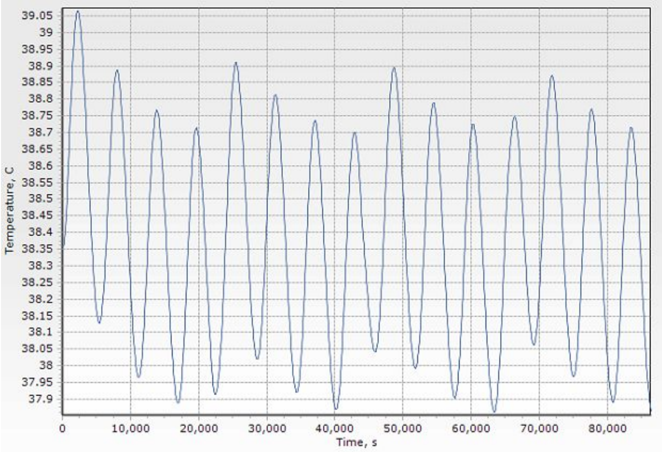
Worst Case Cold



Actual Case

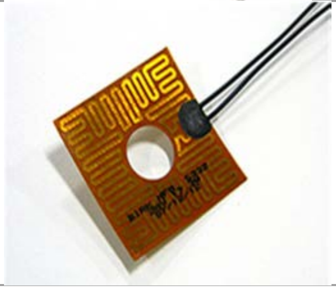


Worst Case Hot



0% Heater Duty Cycle in all 3 cases

Thermal - Components

Component Name	Model	Specifications	Image
Resistive thermal detectors (RTD)	Littelfuse PG102A1	-50°C ~ 500°C ±0.15°C	
Battery Heaters	BK3514-57.4-L12-E02	3.8W Peak	
Thermal Coatings	5 mil silver-teflon coatings on +Y,-Y,-X panels		

Thermal - Requirements Compliance

Req.	Description	Compliance
TCS-1	The subsystem shall maintain all components within operational temperature limits during Normal Operations Mode	Compliant - All components are within their operational temperature
TCS-2	The subsystem shall maintain all components within survivable temperature limits for mission duration	Compliant - All components are within their survival temperature.

Thermal - Next Steps

- Recent fastener changes needs to be reflected in the thermal model.
- Heatloads/Materials properties are unknown for some of the payload components. The model has to be updated once those are known.
- Reflect future changes(if any) made in CAD to thermal model.
- Testing Procedure document for thermal testing

Thermal - Testing

1. Thermal Vacuum Testing (TVAC)
    a. TVAC cycle testing consists of several hot and cold periods with the spacecraft in operation while in a vacuum environment.
    b. This stresses the system in an environment that is much more flightlike than bench testing.
2. Thermal Balance Testing (TBAL)
    a. TBAL testing has a similar test configuration toTVAC cycling, but it instead strives to reach thermal equilibrium in hot and cold cases to have a steady-state configuration to directly compare a thermal model with measurements.
    b. Ideally, these will be the worst-case hot and cold on-orbit environments.
    c. TBAL results would help to fine tune the parameters used in thermal desktop to produce more accurate results.

EPS: Solar Panels and Batteries

Ryan

Power Budget

		Spacecraft Subsystem, Unit, Quantity and Power Consumption							
Subsystem	Component/ Use Case	Max Voltage (V)	Max Current (A)	Peak Power (W)	Nominal Power (W)	Contingency (%)	Qty	Total Peak Power (W)	Total Nominal Power (W)
CDHS	Board/Wire	3.3		0.91	0.64	5	1	0.9555	0.672
COMMs	Astrodev UHF Radio TX	12		3	0.2	5	1	3.15	0.21
	espace HSTX S-Band Radi	12		5	0.9	5	1	5.25	0.945
ADCS	XACT/RW (25%)	12		2.47	0.00	5	1	2.5935	0
	XACT/RW+TR	12	2.53	2.82	0.00	5	1	2.961	0
	XACT/RW (10%)	12		1.92	0.00	5	1	2.016	0
EPS	Board/Wire	-	-	0.1	0	5	1	0.105	0
Thermal	Heaters	14.8 Batt		3	0	25	1	3.75	0
	Sensors	3.3		0.1	0	25	5	0.625	0
STR	UHF Antenna Deploy	14.8 Batt		1	0	25	1	1.25	0
	Solar panel burn wire	14.8 Batt		1	0	25	2	2.5	0
	E- Field burn Wire	14.8 Batt		1	0	25	4	5	0
	CTD Boom	12	0.1666	2	0	5	1	2.1	0
Payload	EF Pre-Amp	12		0.256	0.256	5	1	0.2688	0.2688
	BF Pre-Amp	12		0.015	0.015	5	1	0.01575	0.01575
	Analog Board	12		2.66	2.66	5	1	2.793	2.793
	Digital Board	12		1	1	5	1	1.05	1.05
GPS	Board/Wire	3.3	6	1	0	5	1	1.05	0

Power Budget

Subsystem	Component/ Use Case	Normal Ops. (Sun Pointing)				Downlink Ops. (Sun Exposed)				Normal Ops. (Eclipse)				Downlink Ops. (Eclipse)			
		Duty CyclePeak	Nominal	(W)	(%)	Duty CyclePeak	Nominal	(W)	(%)	Duty CyclePeak	Nominal	(W)	(%)	Duty CyclePeak	Nominal	(W)	(%)
CDHS	Board/Wire	40%	60%	0.82362	10%	100%	0%	1.05105	10%	40%	60%	0.82362	10%	100%	0%	1.05105	10%
COMMs	Astrodev UHF Radio TX	10%	90%	0.567	20%	20%	80%	0.861	10%	10%	90%	0.5355	10%	20%	80%	0.861	10%
	espace HSTX S-Band Radi	0%	100%	0.945	20%	100%	0%	5.775	10%	0%	100%	0.945	10%	100%	0%	5.775	10%
ADCS	XACT/RW (25%)	0%	0%	0	20%	100%	0%	2.85285	10%	0%	0%	0	10%	100%	0%	2.85285	10%
	XACT/RW+TR	85%	0%	3.02022	20%	0%	0%	0	10%	85%	0%	2.768535	10%	0%	0%	0	10%
	XACT/RW (10%)	15%	0%	0.36288	20%	0%	0%	0	10%	15%	0%	0.33264	10%	0%	0%	0	10%
EPS	Board/Wire	100%	0%	0.1155	10%	100%	0%	0.105	0%	100%	0%	0.105	0%	100%	0%	0.105	0%
Thermal	Heaters	0%	100%	0	10%	0%	100%	0	0%	20%	80%	0.75	0%	20%	80%	0.75	0%
	Sensors	100%	0%	0.6875	10%	100%	0%	0.6875	10%	100%	0%	0.6875	10%	100%	0%	0.6875	10%
STR	UHF Antenna Deploy	0%	100%	0	10%	0%	100%	0	0%	0%	100%	0	0%	0%	100%	0	0%
	Solar panel burn wire	0%	100%	0	10%	0%	100%	0	0%	0%	100%	0	0%	0%	100%	0	0%
	E- Field burn Wire	0%	100%	0	10%	0%	100%	0	0%	0%	100%	0	0%	0%	100%	0	0%
	CTD Boom	0%	100%	0	20%	0%	100%	0	0%	0%	100%	0	0%	0%	100%	0	0%
Payload	EF Pre-Amp	0%	100%	0.2688	10%	0%	0%	0	0%	0%	100%	0.2688	0%	0%	0%	0	0%
	BF Pre-Amp	0%	100%	0.01575	10%	0%	0%	0	0%	0%	100%	0.01575	0%	0%	0%	0	0%
	Analog Board	0%	100%	2.793	10%	0%	0%	0	0%	0%	100%	2.793	0%	0%	0%	0	0%
	Digital Board	0%	100%	1.05	10%	0%	100%	1.05	0%	0%	100%	1.05	0%	0%	100%	1.05	0%
GPS	Board/Wire	100%	0%	1.26	20%	100%	0%	1.155	10%	100%	0%	1.155	10%	100%	0%	1.155	10%
Totals				11.90927				13.5374				12.230345				14.2874	

Battery Overview

Tenergy Li-Ion 18650

- 14.8 V
- 2600 mAh
- Includes charge protection

Based on Worst Case Orbit Analysis

- Longest expected eclipse, downlink
- Need **22.12 Whr** capacity (EOL)
    - 60% SOC requirement

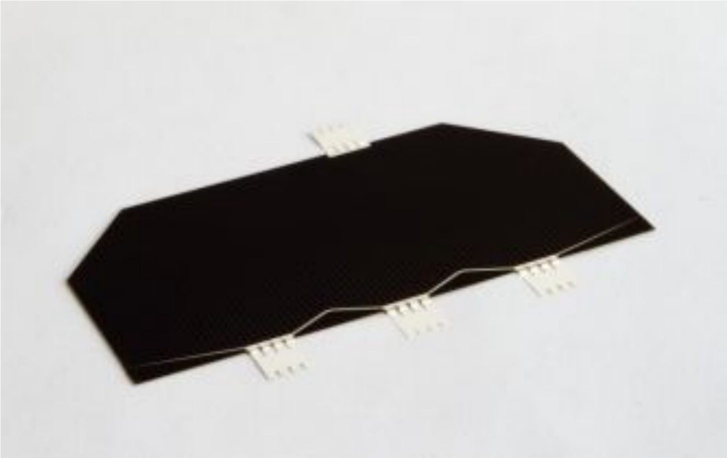
Design

- 2 Tenergy batteries
- **76.96 Whr** (BOL)
- **61.57 Whr** (EOL)
    - Meets **KDR EPS-2**,The subsystem battery shall be able to provide a minimum capacity of 11.23 Whr (TBR)
- **178%** margin (EOL)
    - Assuming 20% battery degradation
    - Two batteries for redundancy

Solar Panel Overview

Azur Space Solar Cells

- EOL efficiency of 26.6%
- 3.56 g/cell
- 30.18 cm^2/cell



Based on Worst Case Orbit Analysis

- Shortest sun exposure time
- Need **22.54 W** generation (EOL)
  - 90% PPT
  - 15 deg off-point angle

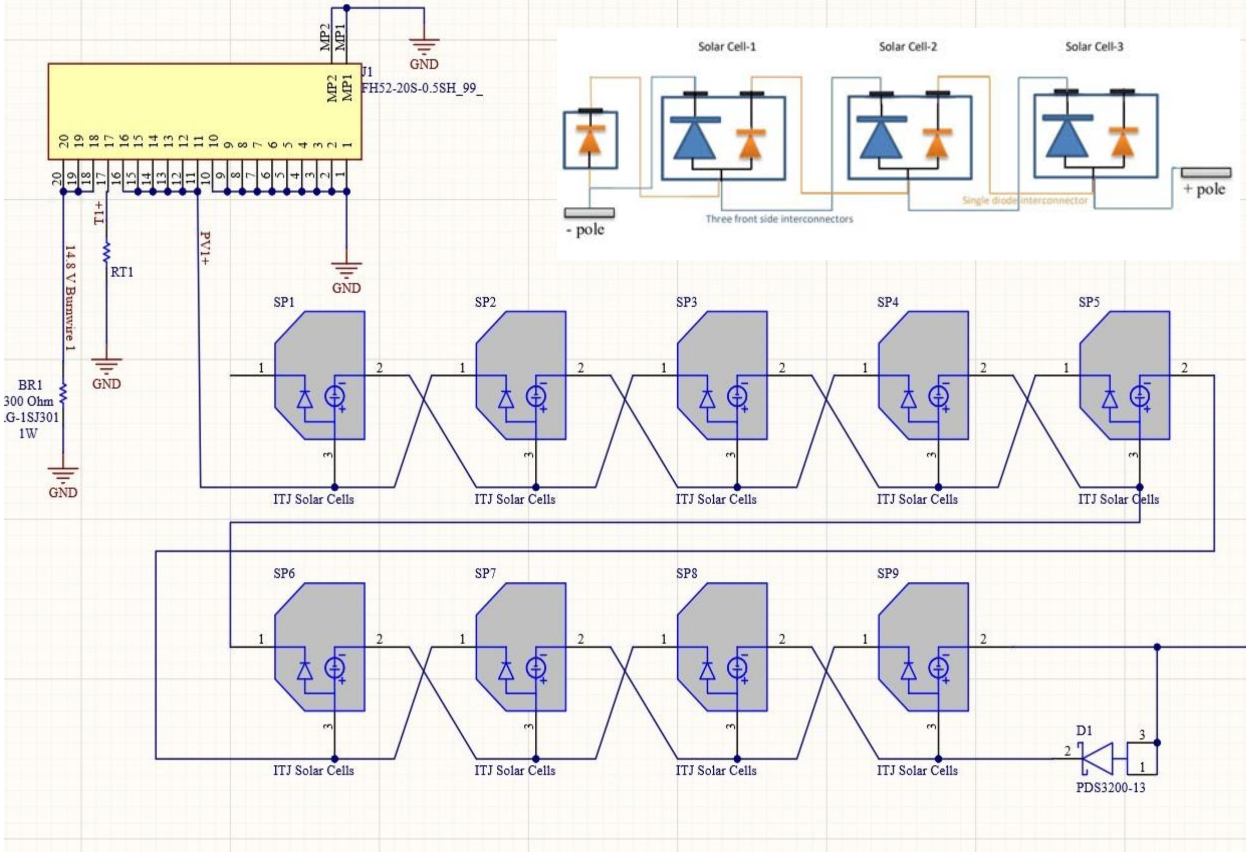
Design

- 27 solar cells, 9 per string for 21.15V
- **25.63 W** (EOL)
  - Meets **KDR EPS-4**,The subsystem shall be able to provide 25.2 W (TBR) EOL to the spacecraft
- **14%** margin
- Based on MinXXS Heritage

EPS: Solar Panels & Battery - Key Requirements

Req.	Description	Reasoning
EPS-1	The subsystem shall be power positive on average over the course of an orbit	If the spacecraft isn't power positive during these phases it will likely discharge the battery to its lowest capacity and cause the spacecraft to die prior to the end of the planned mission duration.
EPS-2	The subsystem battery shall be able to provide a minimum capacity of 22.12 Whr	The battery must have a capacity that holds enough charge to assure that the spacecraft will be powered through eclipse.
EPS-2.1	The subsystem battery shall not fall below a depth of discharge of 60%	The battery shall not fall below 60% SOC during any point during the mission due to the large number of cycles
EPS-4	The subsystem shall be able to provide 22.54 W EOL to the spacecraft	Must be able to provide enough power production for battery recharge following eclipse and/or downlink (During Sun Time)
EPS-11.8	All flight cells and battery packs shall be subjected to an approved set of acceptance screening tests to ensure the cells will perform in the required load and environment without leakage or failure.	Ensures required power generation is met and cells and batteries function and perform in the required environment
EPS-11.13	For battery designs greater than 80 Wh energy employing high specific energy cells (greater than 80 watt-hours/kg, for example, lithium-ion chemistries) require additional assessment by NanoRacks due to potential hazard in the event of single-cell, or cell-to-cell thermal runaway.	We cannot launch if we do not meet the requirements set out in the NRCSD IDD

EPS: Solar Panels - Status



Solar Panel Schematic

- 20 Pin FH52 connector
  - Operating Temperature: **-40°C ~ 105°C**
  - Current Rating: 0.3 A - 0.5A
  - 0.5mm pitch
  - Low profile surface mount
- Pin Assignment
  - Solar Panels: **6 Pins** (PV1+)
    - BOL: 0.448 A
    - EOL: 0.403 A
  - Burnwire Resistor: **3 Pins**
    - 0.049A (0.73W)
  - Thermal Resistor: **1 Pins** (T1+)
    - 0.0148 A
  - GND: **10 Pins**
  - Mounting Pins
    - GND

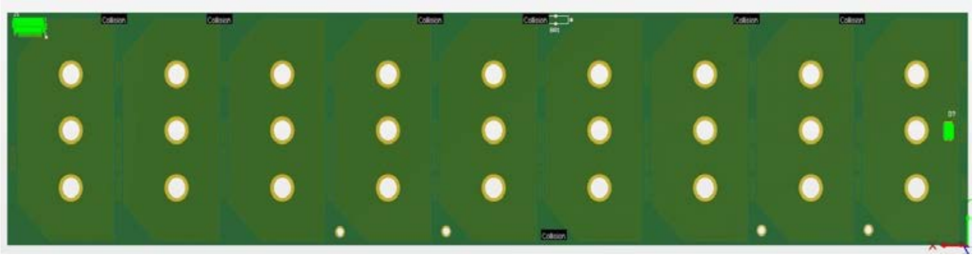
EPS: Solar Panels - Status - Layout and Dimension

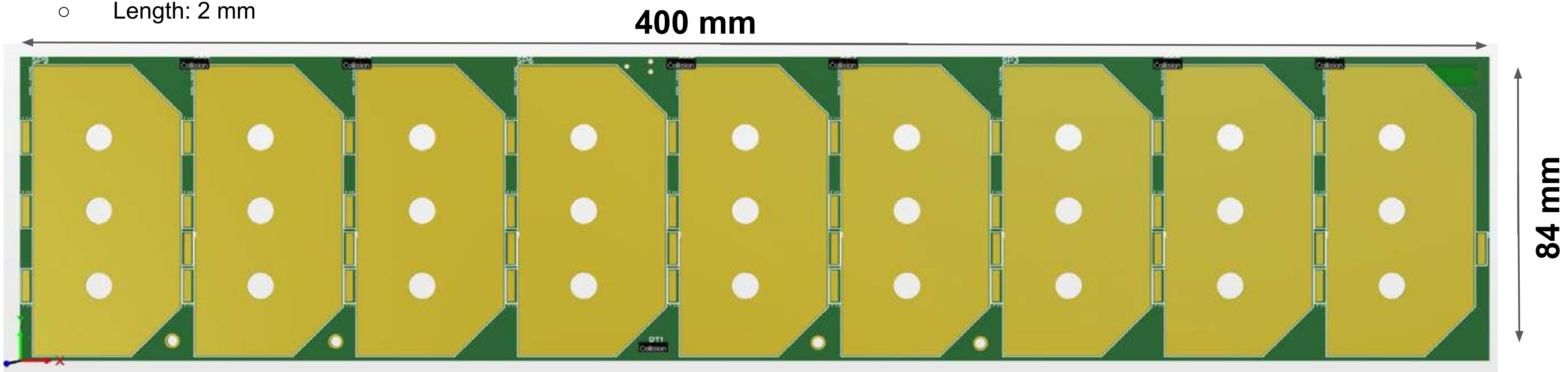
Hinge Mounted

Solar Panel PCB Design
- Largely influenced by MAXWELL and MinXXS Design
- Decoupled Design

Burnwire Location
- 228mm

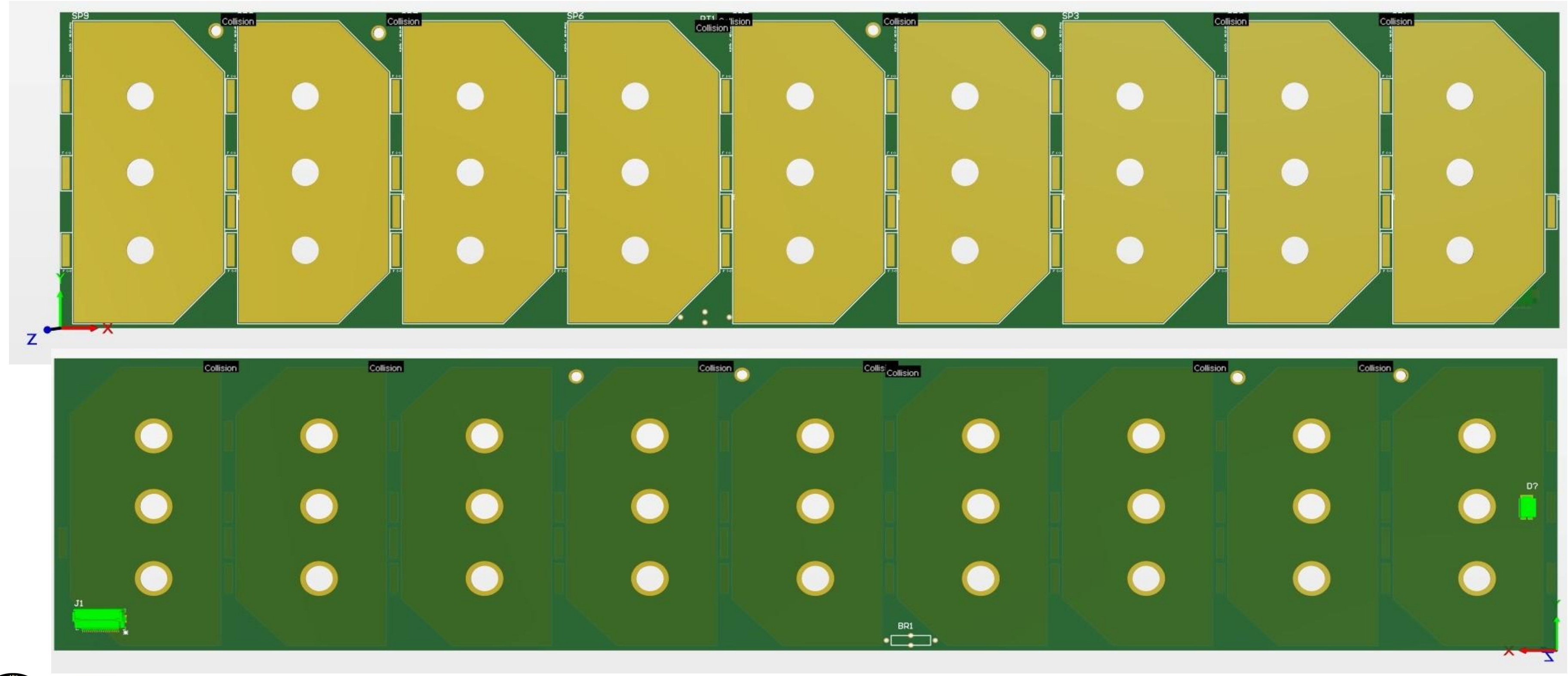
Solar Cell Spacing and Pad Sizing
- Spacing between cells(not including the interconnectors): 4 mm
- Interconnector Dimensions:
  - Width: 6.5 mm
  - Length: 6.63 mm
- Pad Dimensions:
  - Width: 8.6 mm
  - Length: 2 mm





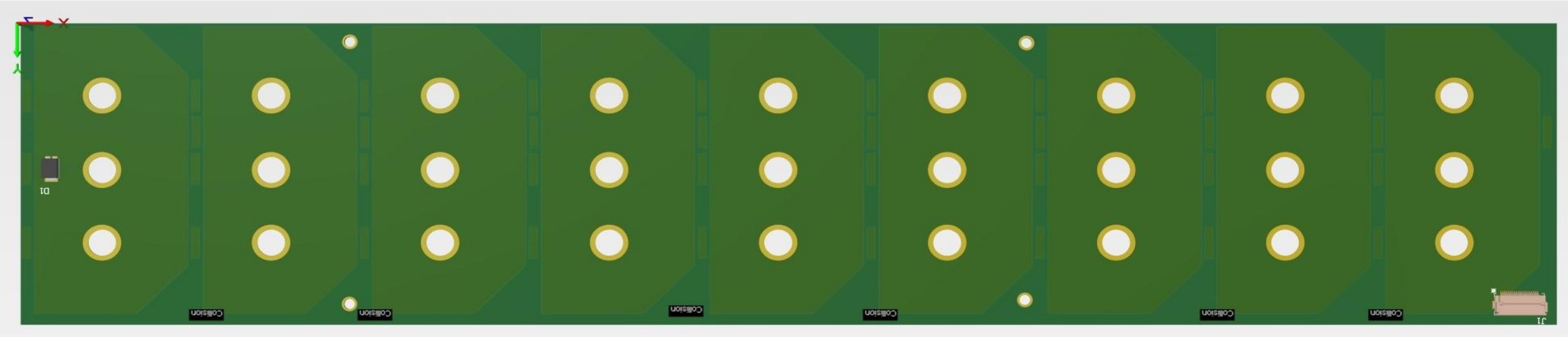
EPS: Solar Panels - Status - Layout and Dimension

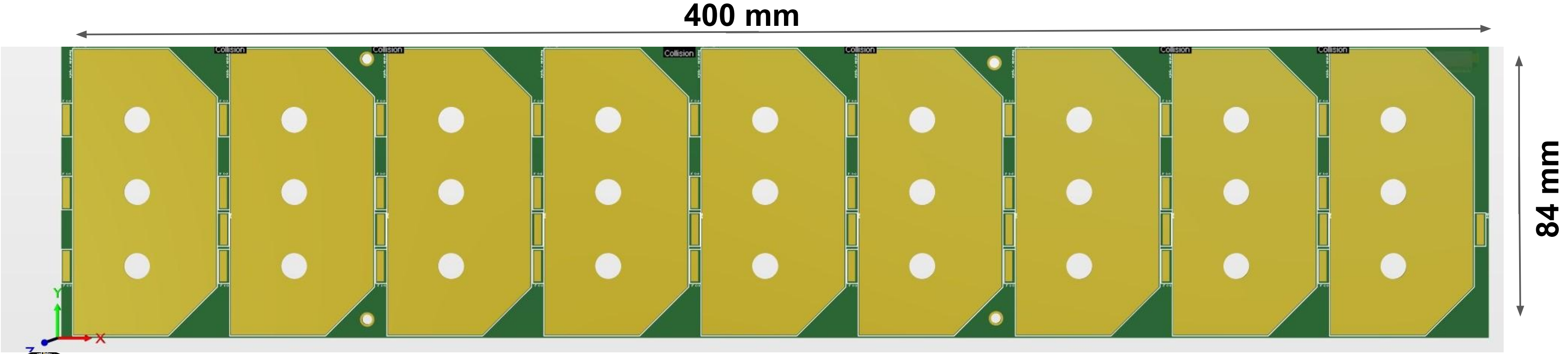
Hinge Mounted



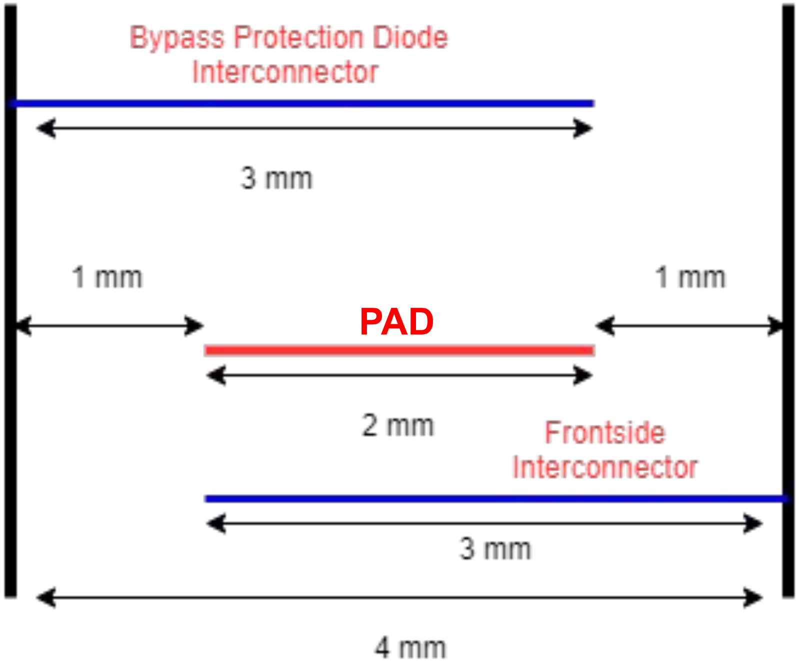
EPS: Solar Panels - Status - Layout and Dimension

Body Mounted





EPS: Solar Panels - Status - Interconnectors



Sizing

- Due to the size constraint on CANVAS the interconnector will need material with a diameter of 2.3mm to complete the bend to ensure contact with the PCB and alleviate the need to trim the interconnectors
    - Interconnectors can be trimmed and will not affect the functionality of the solar cell

EPS: Solar Panels - Next Steps

PCB - Altium

- Complete Routing (2 days)
- Fix Silkscreen Collisions (1 day)
- Standoffs (Locations and Amount) (1-2 weeks)
- Mounting holes for plexiglass to be fastened to the top of the PCB to protect board during handling (Remove Before Flight)
- Ensure Schematics are easily followable (2-4 days)

Manufacturing

- Finalize manufacturing document (1-2 weeks)
  - List new steps to be taken given the layout change
  - Create a materials list
- Layout Review (1-2 weeks)
- Get board ready for production(1-2 months)
  - Export Gerber files
  - Check Gerber files with Advanced Circuits
  - Create BOM and order components
- Manufacture Board (1-week)

Testing

- Create test plans/procedures for each individual test (1-3 months)
- Complete Series of Tests (1-4 months)

EPS: Solar Panels - Next Steps

Testing

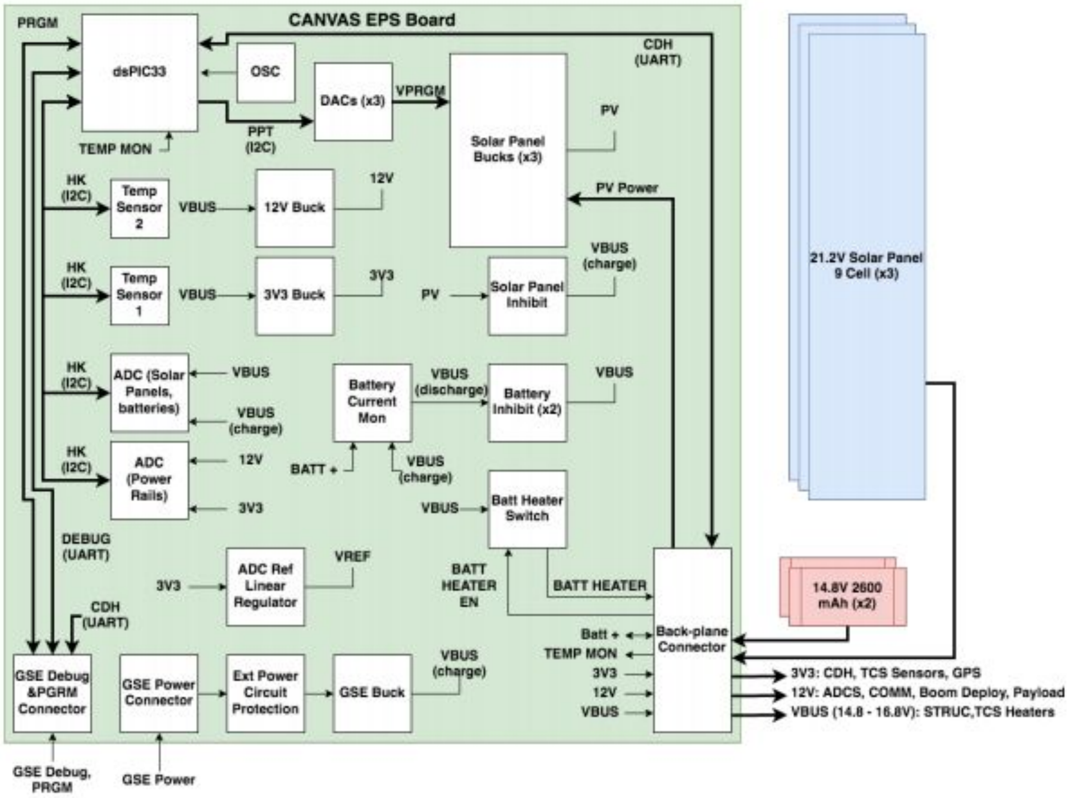
- Thermal Vacuum Test (TVAC)
  - Determine panel performance in a space-representative thermal and vacuum environment
    - Run hot and cold cycles
- Solar Panel Glow Test
  - Ensure each solar cell has no defects
- Burnwire Resistor/Deployment Test
  - Test burnwire resistor (fishing line, binder clip, and power supply)
  - Solar Panel Deployment after assembly
- Outdoor Test
  - Cloudless day to confirm panels are producing the expected amount of power

EPS Board

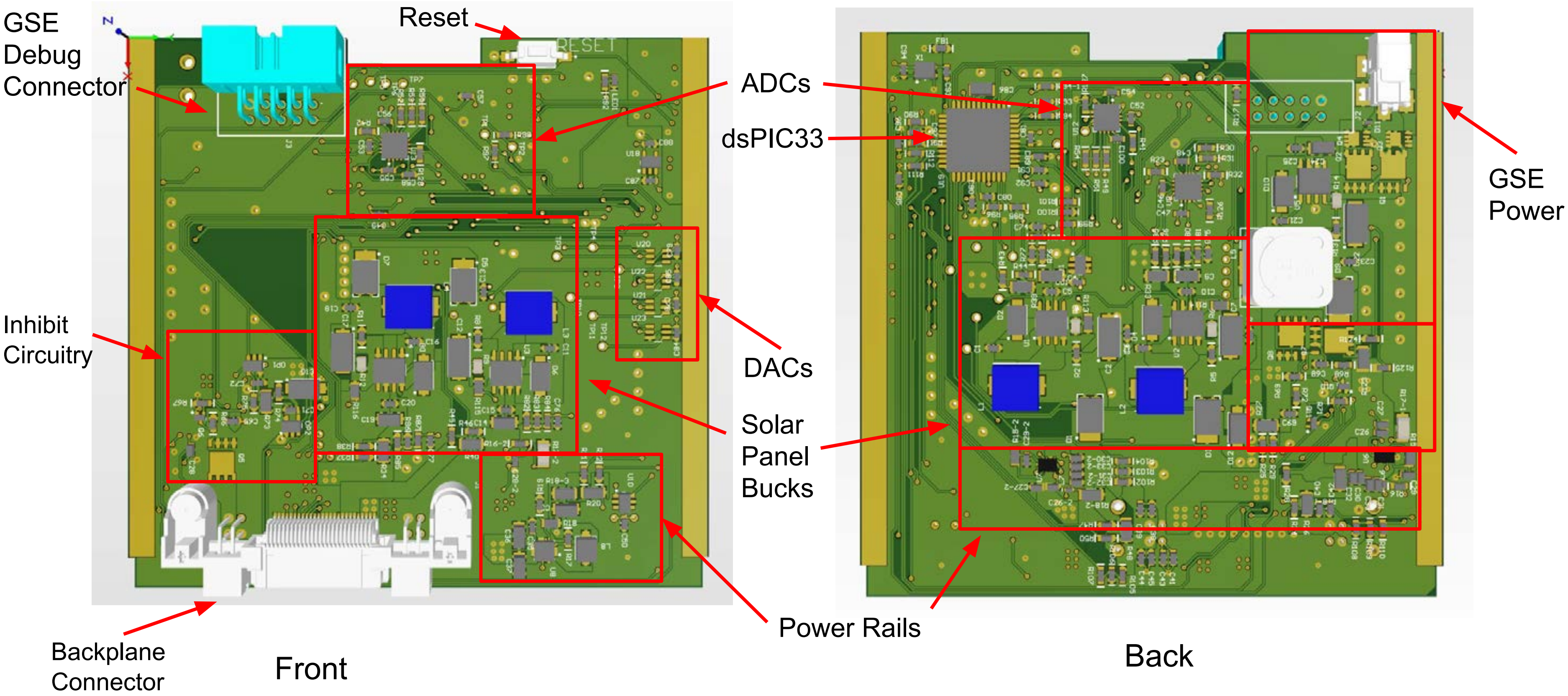
Jett

EPS Board - Overview

- Power Management board
- Based on MAXWELL Heritage
- 3.3V, 12V regulated rails
- Dedicated 12V rail for XACT
- 14.8-16.8V bus voltage
- Up to 4 solar panel inputs
- Altered to 90x93mm
- I2C Housekeeping line used for voltage monitors and on board temperature sensors



EPS Board - Overview



Overview | Key Reqs | System Status | Next Steps

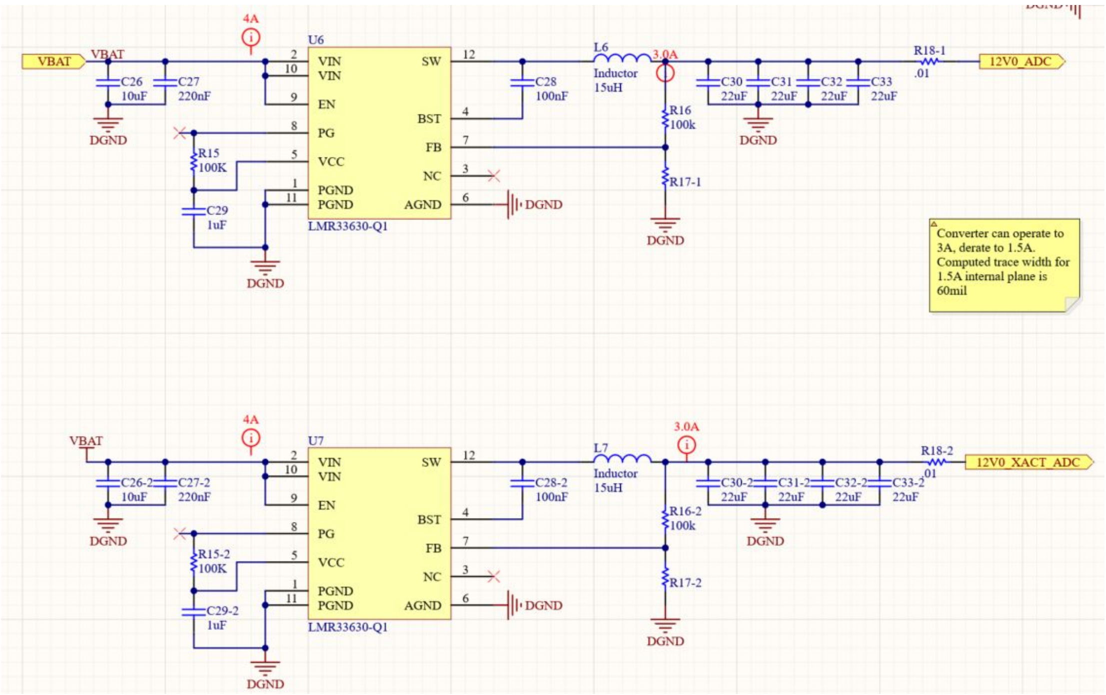
EPS Board - Key Requirements

Req.	Description	Reasoning
EPS-12	The EPS PCB shall conform to a 90x94 form factor	The PCB must fit within the bus without alterations to the structure
EPS-13	The EPS PCB shall be compatible structurally and electronically with a backplane connector	The structural design solution encompasses a backplane along the -Y bus panel to meet volume requirements for the PCB assembly
EPS-6	The EPS shall provide power to every subsystem at the appropriate voltage	The EPS must provide voltages that are required by each subsystem and its specified components
EPS-11	The EPS subsystem shall follow all electrical system requirements of the dispenser.	Must meet Nanoracks dispenser requirements.

EPS Board - Changes from MAXWELL

- Updated remaining sheets and nets to account for 12V instead of 5V.
- Swapped supporting electronics for the solar panel buck converter. The buck converter, TPS5420, was adjusted to output 16.8V instead of MAXWELL's 14.6V.
- Adjusted voltage divider for analog measurement of solar panel voltage used in peak power control loop (net called PVx PIC in schematics).
- Added 1 more solar panel temperature sensors.
- Add SP3 + to PIN 1
- Adjusted housekeeping voltage dividers for analog measurement of 5V0 to 12V0.
- Resized board dimensions from 111.76 x 93.98 x 15 (mm) to 90 x 93 x 15 (mm).
- Removed inhibit circuitry

EPS Board - System Status



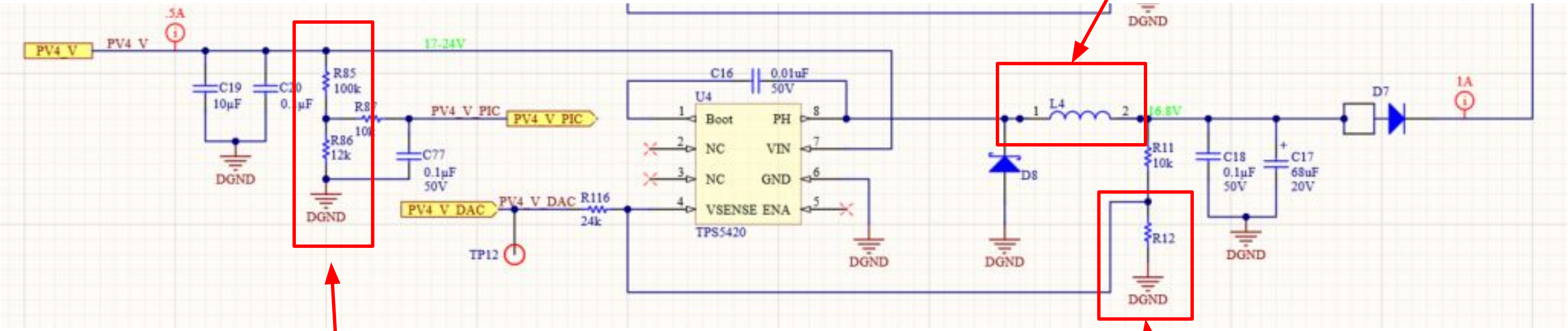
- Same buck converter for universal 12V line.
  - Same surrounding circuitry
- Additional converter needed for XACT current draw.

EPS Board - Solar Panel Bucks

Vout = 16.8V
Vin(Max) = 24V
Kind = .2
Fsw = 500 kHz

Iout = 1A
Lmin = 63 µH
Lused = 68 µH

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW} \times 0.8}$$



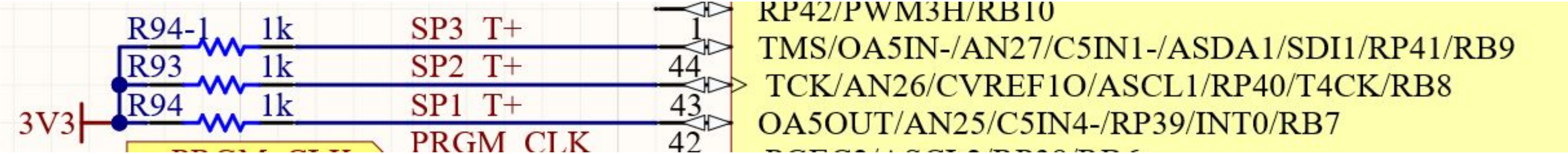
Voltage Divider
R1 = 100 kΩ
R2 = 12 kΩ
Vinmax = 24V
Voutmax = 2.57V

R1 = 10 kΩ
Vout = 16.8V
R2 = 783.7Ω
Rused = 787Ω

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221}$$

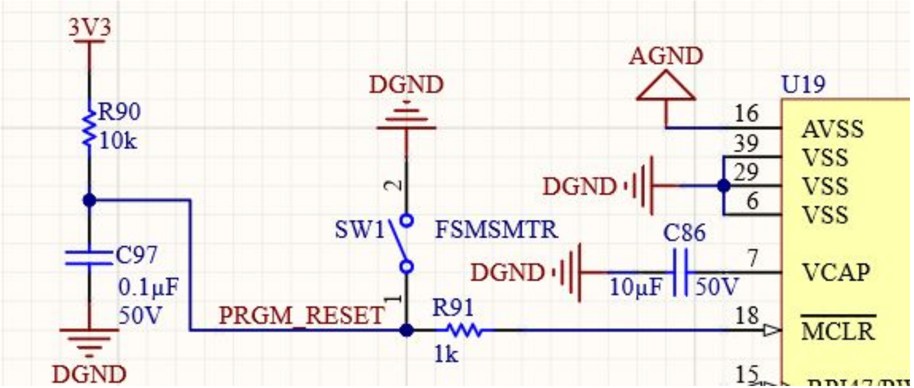
EPS Board - Solar Panel Temperature Sensors

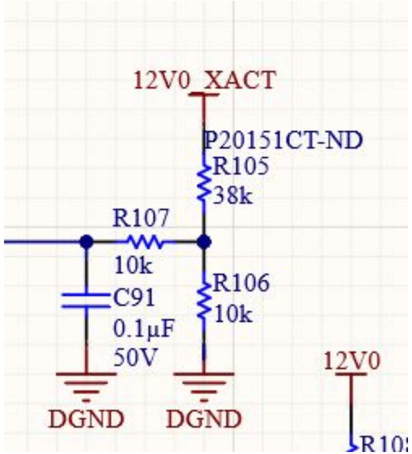
- 3 Solar Panel Sensors
- Enough for the 3 solar panel strings
- Simple voltage divider for TFPT1206L1001DV thermoresistors (1kΩ resistance)
- At 25°C Voltage seen by pic is 1.65V



EPS Board - System Status

- Physical button added to program restart for testing
  - Should be unpopulated for flight board

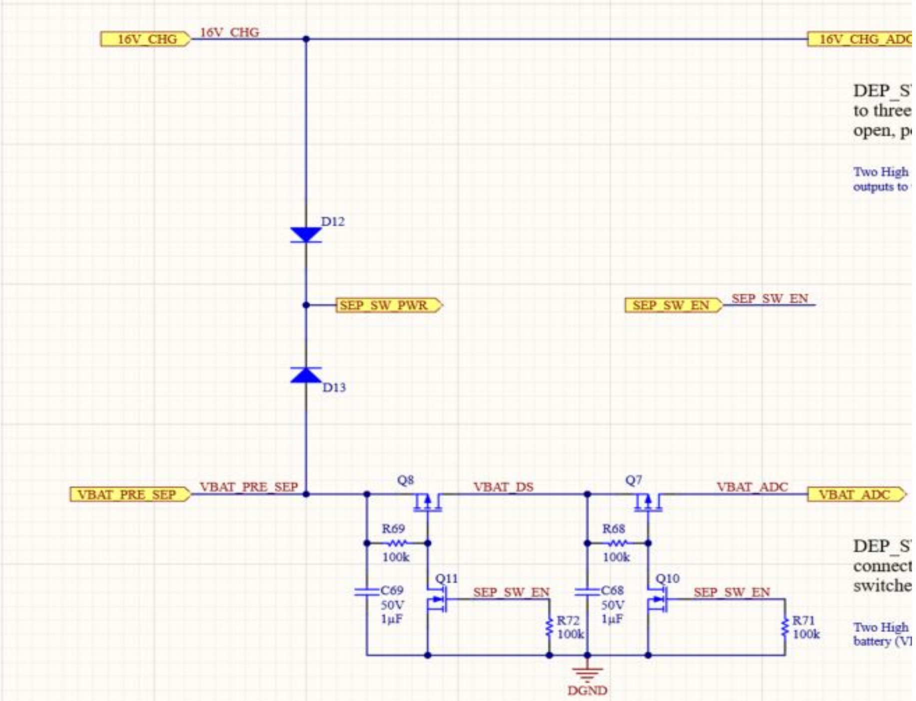


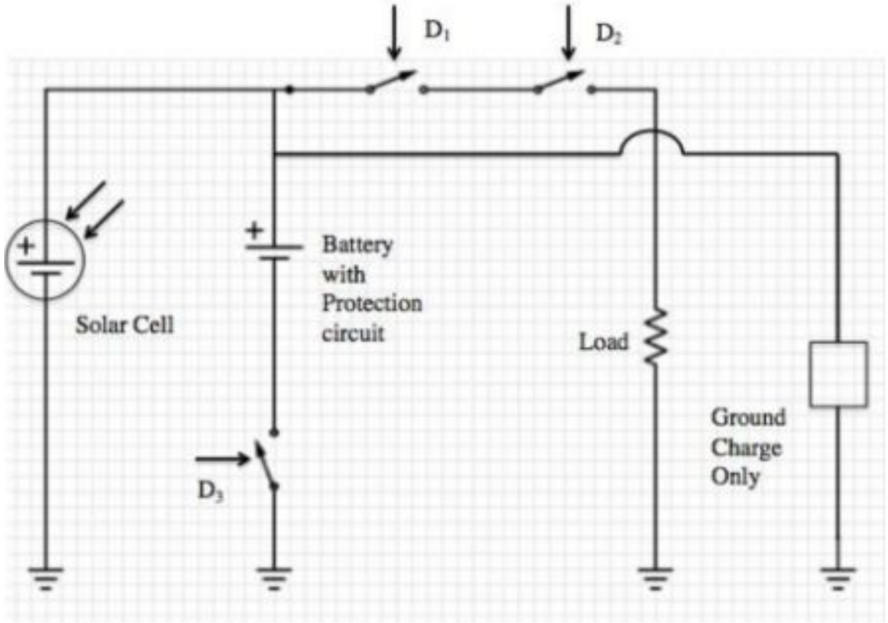


Voltage divider adjusted for 12V instead of 5V. **2.5V** output to PIC.

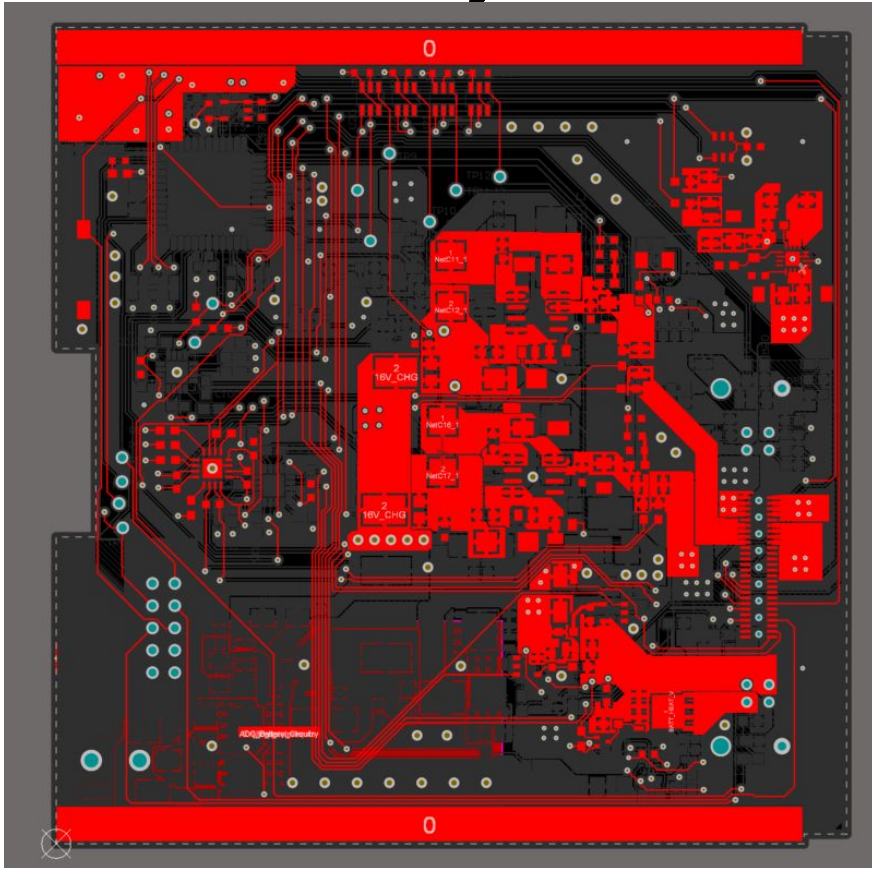
EPS Board - Inhibit Circuitry

- Removed solar panel inhibits.
- Deployment switches on backplane.
- Two connected to “SEP_SW_EN” Net.

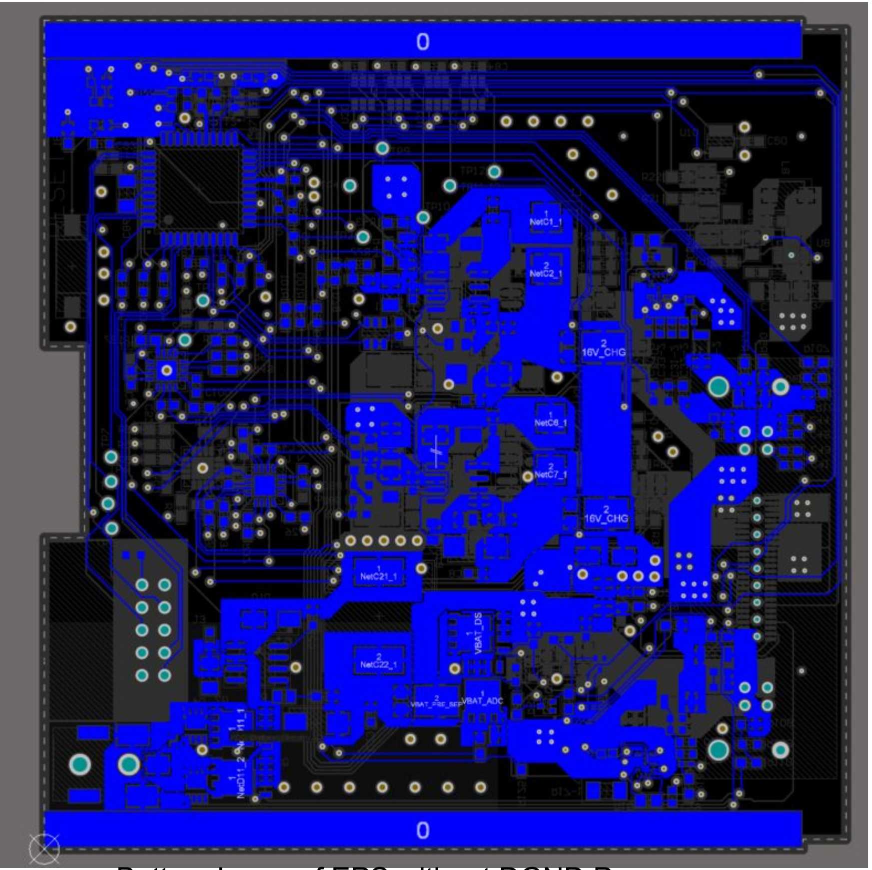




EPS Board - Layout



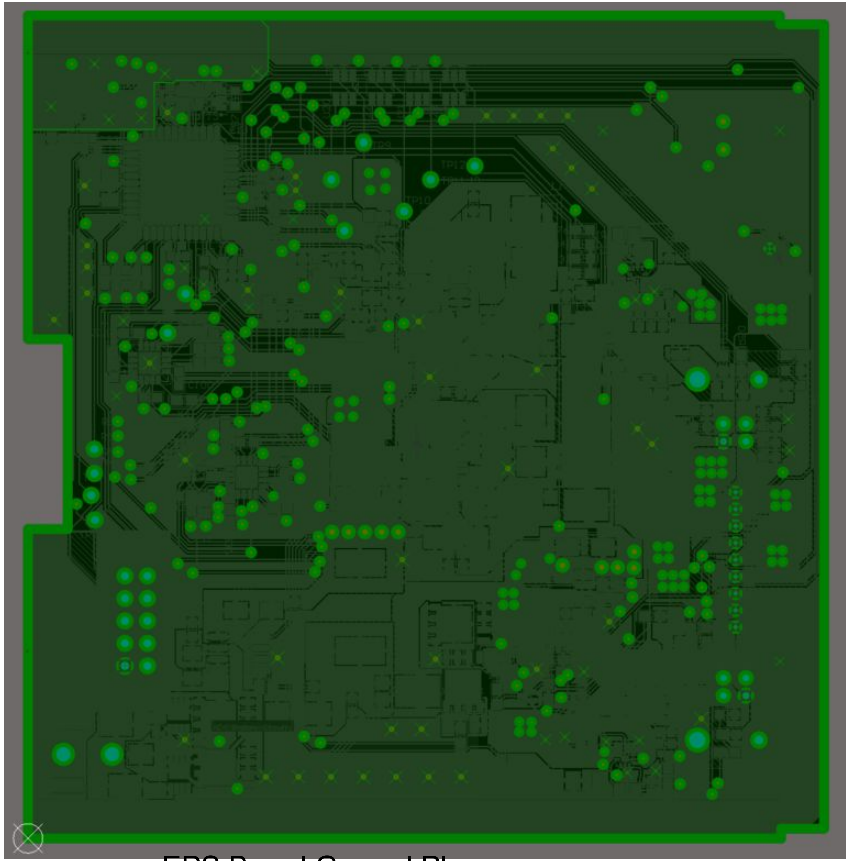
Top Layer of EPS without DGND Pour



Bottom Layer of EPS without DGND Pour

EPS Board - System Status

EPS Board Power Plane



EPS Board Ground Plane

EPS Board - Next Steps

- Clean up schematics for easier readability(1 week)
- Get board ready for production(2 weeks)
  - Export Gerber files
  - Check Gerber files with Advanced Circuits
  - Use Altium to create BOM and order components
- Procure Board(2 weeks)
- Populate board(1 month)
- Coordinate with FSW to adjust software

EPS Board - Testing

- EMI testing for batteries, solar panels, power management PCB
  - Verify MR-2: 5 nT requirement for magnetic field measurements
- Battery charge and discharge tests
  - Verify EPS-1.1: 70% SOC requirement
- Battery temperature tests
  - Verify TCS-2: keep components within operational limits
- EPS board supply voltage test
  - Verify EPS-4: power distribution to subsystem requirements
- EPS board inhibit switch test
  - Verify EPS-5: NanoRacks requirements, specifically inhibits between battery and ground, and battery and the spacecraft
- EPS board supply switch test
  - Verify EPS-7.2: enable power toggling

Command and Data Handling Subsystem

Chadd

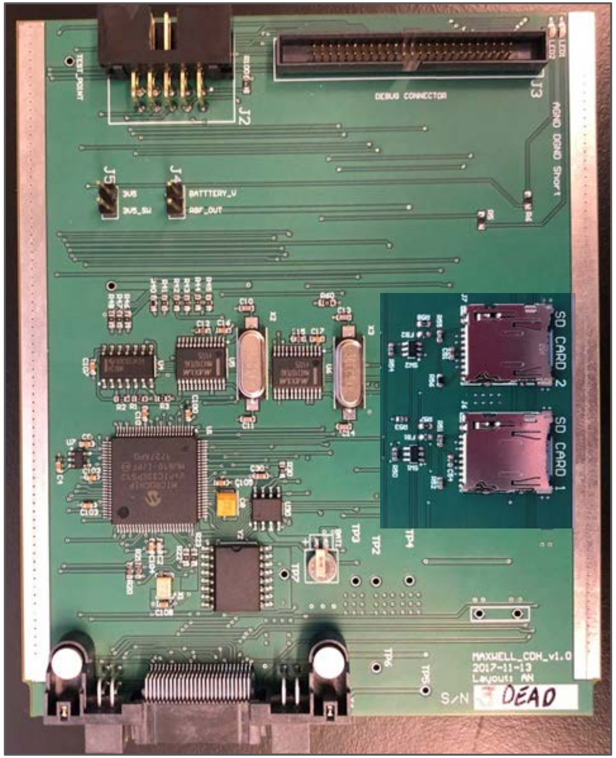
CDH - Overview

CDH?

- PCB with the brains of the spacecraft (MAXWELL ← QB50 Design)
- Microcontroller (OBC)
- Memory
- Interfaces with every subsystem

Functions:

- Runs the Flight Software (FSW)
- Routes commands and data around the spacecraft
    - *Very little* computation done here



MAXWELL CDH

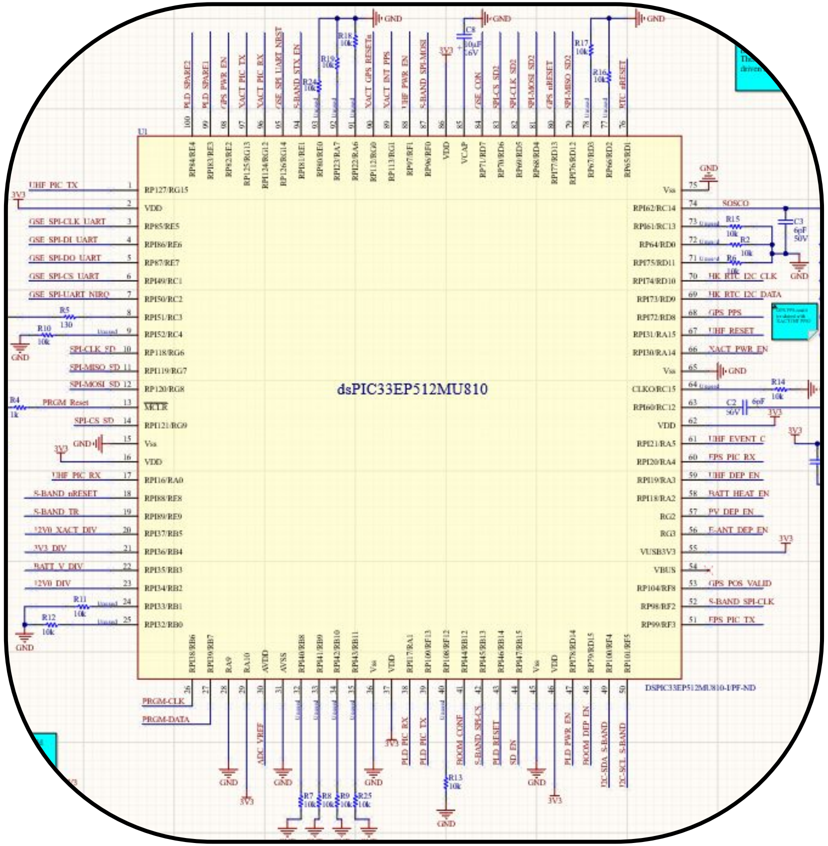
CDH - Overview

Subsystem Status:

- Redesign decisions made for interfacing to COSMO/CANVAS
  - Communication protocols, memory chosen
- Schematic Redesign complete (Internally reviewed)
- Layout Redesign draft complete (pre-Review)

Next Steps

- Layout Review
- Goal: PCB is designed completely and confidently, ready to order



CDH - Key Requirements

Req.	Description	Reasoning
CDH-9,10,11,12	The CANVAS CDH shall be capable of interfacing with all spacecraft subsystems and components.	The CDH must be able to interface to communicate commands and data.
CDH-15	The CDH PCB shall conform to a 90x94 form factor.	The CDH PCB shall have these dimensions in order to fit into the CANVAS card cage
CDH-3	The CDH shall include a minimum of two weeks worth of on board data storage.	Should communications have a recoverable failure, the spacecraft will still be able to record data for a period while the recovery is executed. Two weeks is based off of advice from LASP.

CDH - System Status: PDR Design

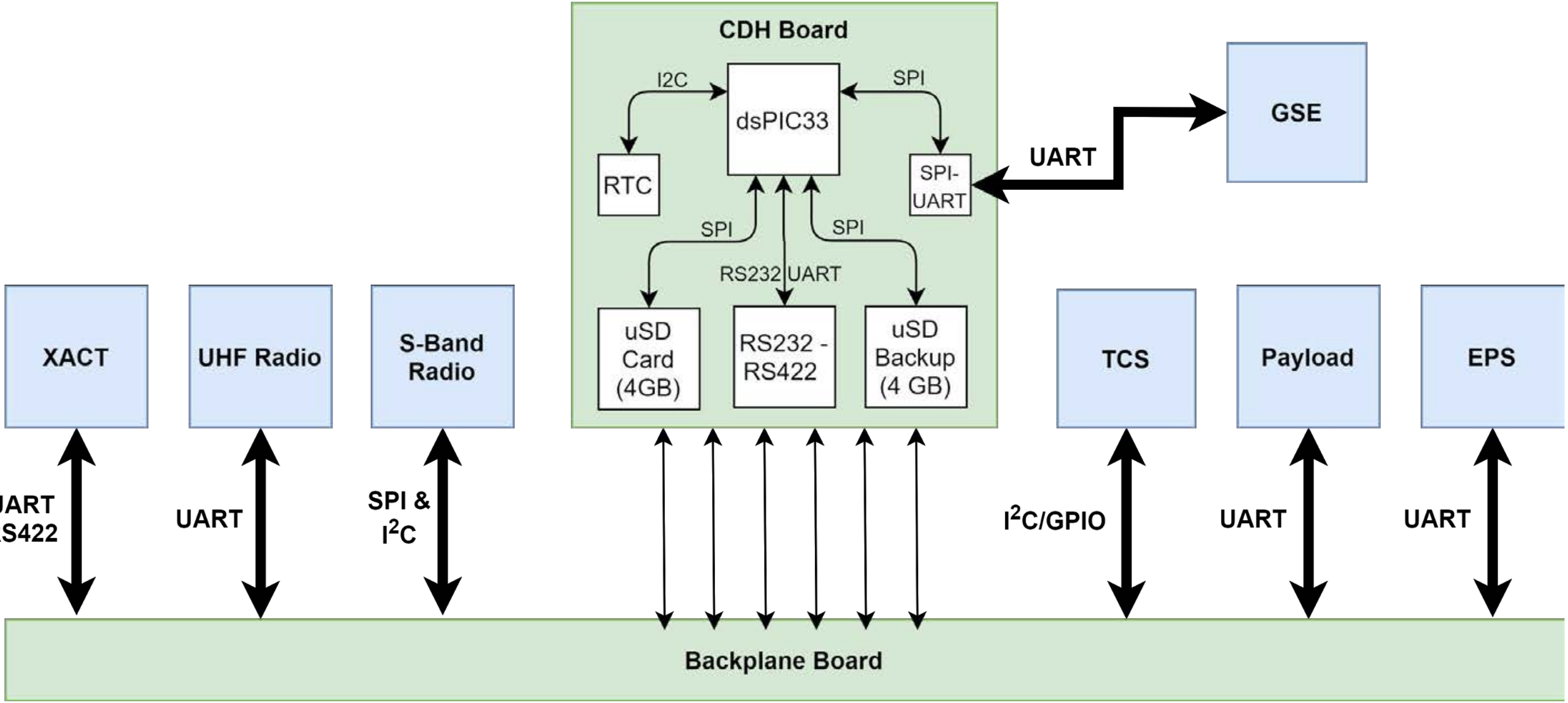
Original Design: MAXWELL

- Microchip Microcontroller dsPIC33EP512MU810
    - 4 UART, 4 SPI, 2 I2C, 2 ECAN (Enhanced Controller Area Network), 1 Parallel Master Port (PMP)
    - 83 remappable I/O pins, including 32 analog capable pins
    - 52 kB RAM
    - 536 kB Program Flash Memory
- 512 byte EEPROM Table Parameter Storage in RTC
- 2 SPI → UART converters
- 2 µSD cards (SPI capable)
- TMP100 Temperature Sensor
- Debug, GSE, and Backplane connectors

CDH - System Status: Redesign

- Added **UART RS 232 → RS 422 Converter** for XACT (TI SN65HVD30MDREP - *new part* - changed from Pre-CDR MAX3162)
- Removal of 1 SPI → UART Converter (**S-Band SPI** becomes a direct line)
- Communication **Protocol Reassignments**
- SD cards retained, parallel development of **NAND Flash** Memory
- New, larger **Backplane** and **Debug** connectors for adequate connector grounding - *new parts*

CDH - System Status: Diagram



CDH - System Status: Memory

Post-PDR Goal: Switch to NAND Flash Memory

- *COSMO's mission was originally thought to be longer with higher radiation exposure*
- *Wanted to avoid MinXSS 2 failure from SEU in µSD control circuitry**

Revised Goal: Investigate feasibility and efficacy of NAND

- *Could NAND Flash be used with our existing architecture?*
- *Is it really better than a µSD card? How much better?*

Findings Summary:

- SLC "Raw" NAND is resistant to SEU and TID, but lacks COTS FTL and ECC
- Managed SLC NAND has the same vulnerable control circuitry as µSD

Final Decision: µSD Critical Path (2 4GB meets KDR 2), NAND Parallel Development

- *Work on NAND development is TBD*

ATP 4GB SLC uSD card

Micron 4GB raw SCL NAND chip

*Hypothesized cause of failure

Memory Comparison V1

CDH - System Status: Communication Assignment

- Interfacing elements considered
  - Number of physical wires
  - Protocol of each connection
  - Function of each connection
- Compared to available CDH pins and protocols
  - 4 SPI “Modules”
  - 4 UART “Modules”
  - 2 I2C “Modules”
    - *These “Modules” can be applied to any of the PIC’s “Remappable Peripheral” pins*

CDH_Interfacing

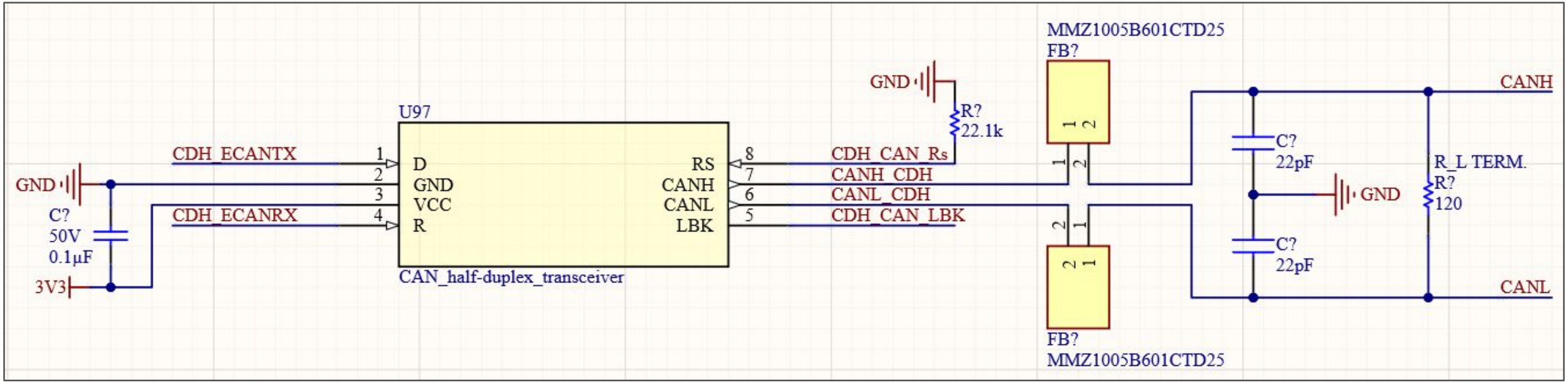
Rev1_CDH_PIC_Redesign_Notes

Protocol	Destination
SPI	S-Band Data
SPI	SD Card 1
SPI	SD Card 2
SPI	SPI-UART GSE
UART	RS232-422 PLD
UART	UHF Radio
UART	EPS
UART	RS232-422 XACT
I2C	S-Band Telem/Command
I2C	Housekeeping/RTC

KDR 1 - Interfacing

CDH - System Status: GPS Interface

- Meeting held end-of-spring to determine need for GPS: Confirmed that it was necessary!
- OEM719 can also communicate with **Controller Area Network (CAN)**
  - Research efficacy and prototype interface - determined possible!
  - 2 CAN translators (one for GPS, one for CDH)



CDH - System Status: GPS Interface

- To avoid CAN testing time and additional hardware driver development time in FSW → communicate *through* XACT
- Plug GPS TX, RX, PPS, GND directly into XACT (we supply 3.3V)
- GPS PPS pass through XACT INT PPS
  - If GPS signal invalid, “freewheel”
- HK is a lot of data! → FSW Discussion:
  - Estimate total HK collected 4-5Hz
  - Easy to put time into PLD packet if we need it.
  - GNC User Guide: can set time collection as “fine” or “course”

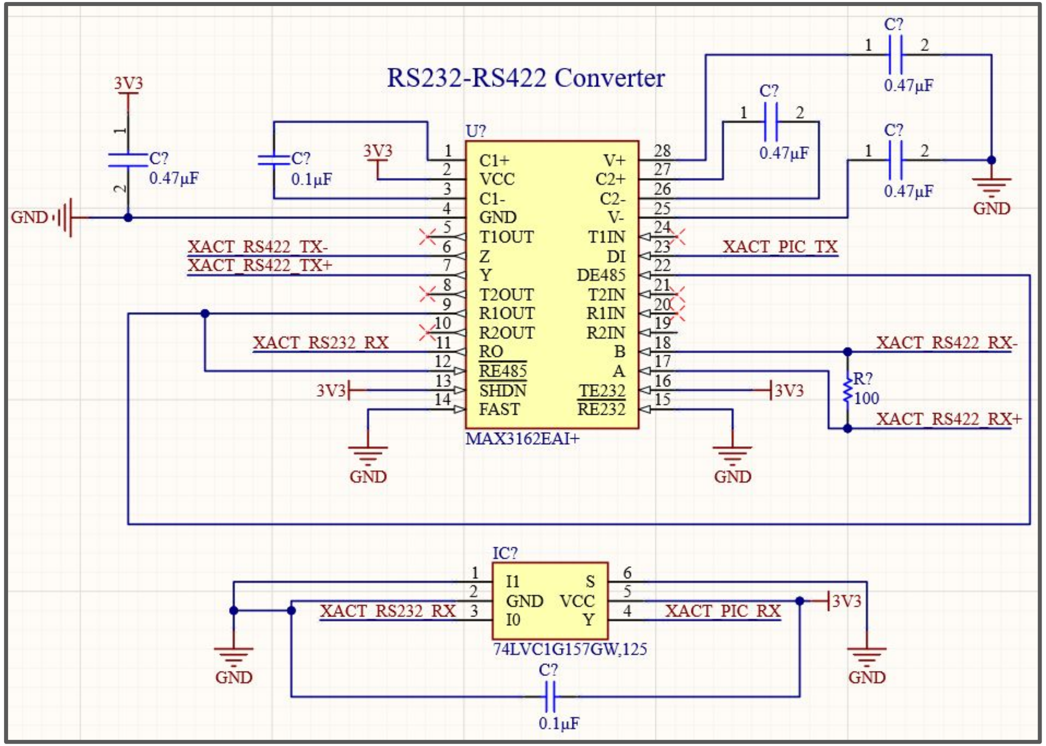
HK Data included in XACT - CDH interface:

GPS TIME
GPS POSITION_ECEF1
GPS POSITION_ECEF2
GPS POSITION_ECEF3
GPS VELOCITY_ECEF1
GPS VELOCITY_ECEF2
GPS VELOCITY_ECEF3
GPS SAMPLE_USEC_CT
GPS CYCLES_SINCE_LATEST_DATA
GPS GPS_LOCK_COUNT
GPS MS_GTRACKED_SATELLITES
GPS MS_GUSED_SATELLITES
GPS MSG_DATA_VALID
GPS GPS_VALID
GPS GPS_ENABLE
GPS NEW_DATA_RECEIVED

CDH - System Status: RS232-RS422 Conversion

XACT ADCS Interface

- Requires RS422 UART connection -- differential voltage protocol
  - TX+, TX-, RX+, RX- and HIGH/LOW signal is measured as difference between these
- dsPIC Microcontroller has digital UART native (not differential)
  - TX, RX, 0V = LOW, 2.5-3.3V = HIGH
- MinXSS design considered
  - MAX3162 test schematic

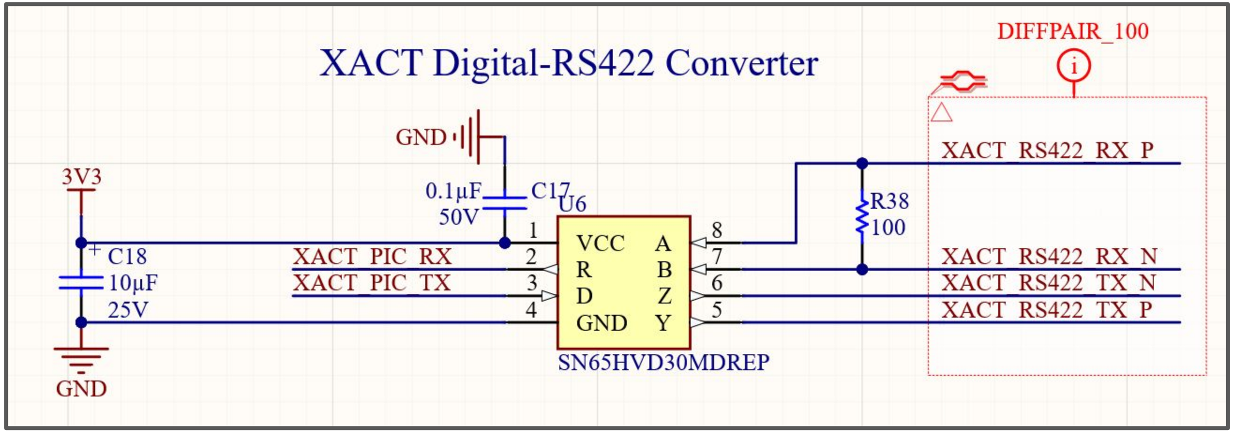


CDH - System Status: RS232-RS422 Conversion

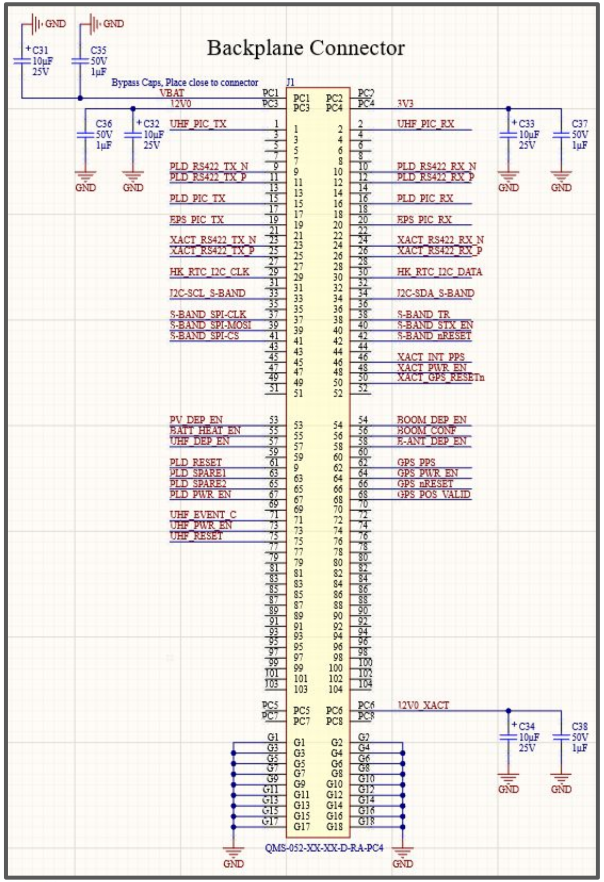
XACT ADCS Interface

- MinXSS design had more capability than required
  - Needed 5V → 3.3V translator to interface with PIC
- Communication with BCT: SVDHVD30 has compatible voltage levels (0V to 2.4-3.3V, differential 2-2.3V)
  - Termination with 100Ω resistor inside XACT
- *Same Translator and schematic used for CANVAS PLD - termination TBD

- Texas Instruments SN65HVD30MDREP:
  - Simple chip, only 8 pins
  - *New Part*, but used at LASP previously
  - No “fragile” charge pumps (fragile to radiation)



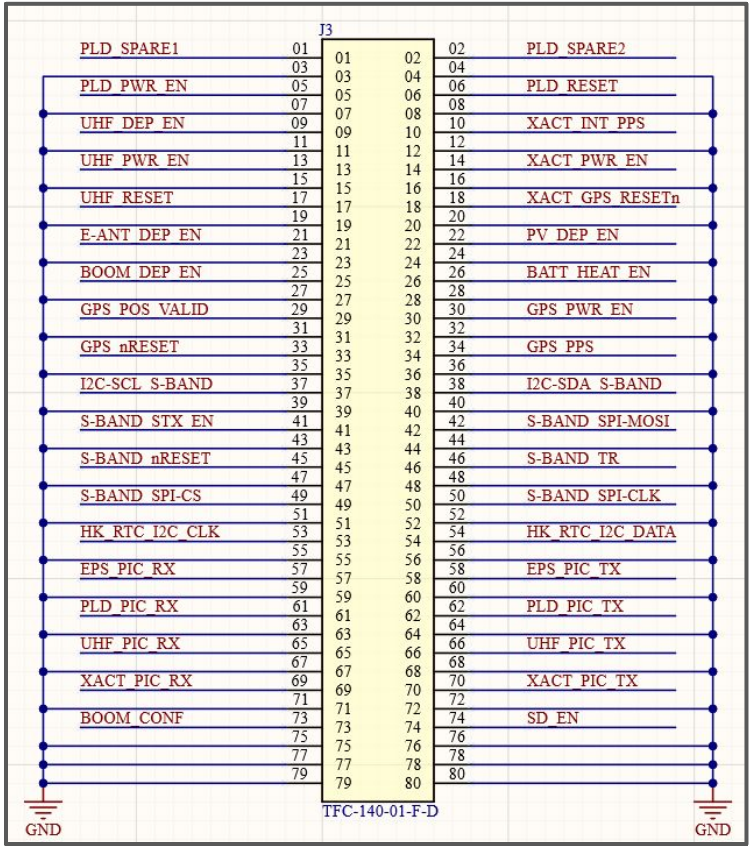
CDH - System Status: Backplane Connector



- Backplane connector supplied in-flight power and signal routing to all subsystems.
- Like signals were grouped together, leaving one pin of ground between communication lines.
- To have sufficient grounding, the connector had to be increased from 52 to 104 pins.
- *NEW PART* - but same part family (QMS-RA) from Samtec - Micro Backplane Systems “Q2™ Rugged/High-Speed Interconnects”

CDH - System Status: Debug Connector

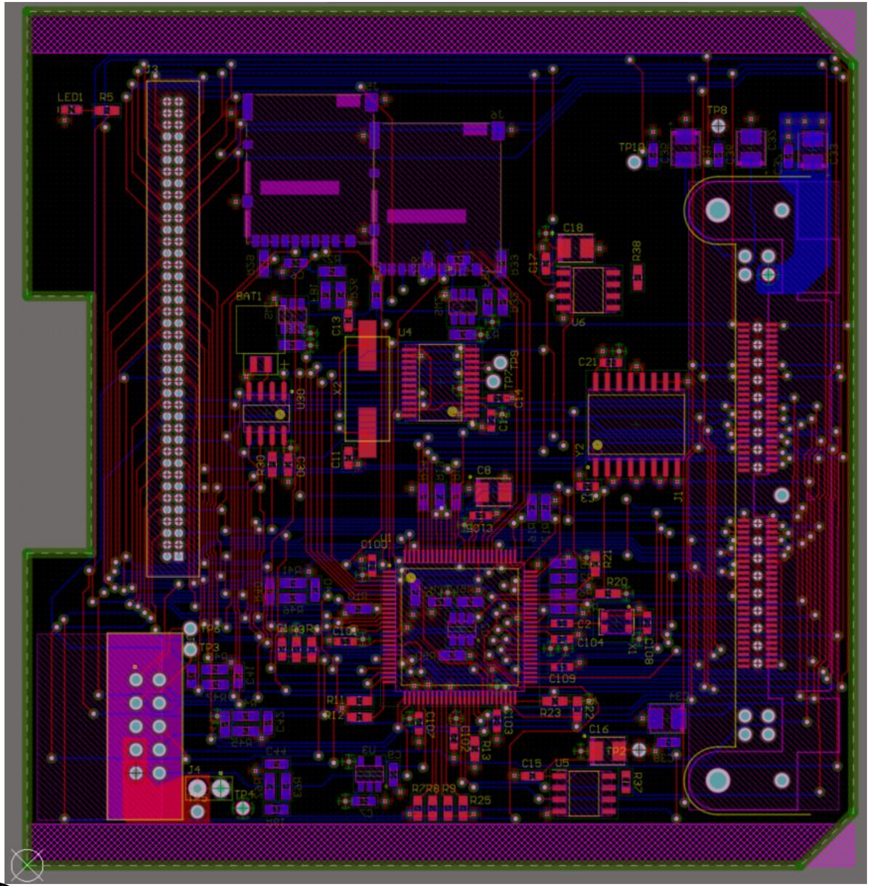
- Debug connector interfaces with the GSE board for table-top testing of CDH functions
- **All** signals were added to the debug connector (excepting differential lines, which cannot be split up)
- To have sufficient grounding, the connector had to be increased from 50 to 80 pins.
- *NEW PART* - but same part family (TFC) from Samtec - 0.050” pitch: “Micro Pitch Board to Board”

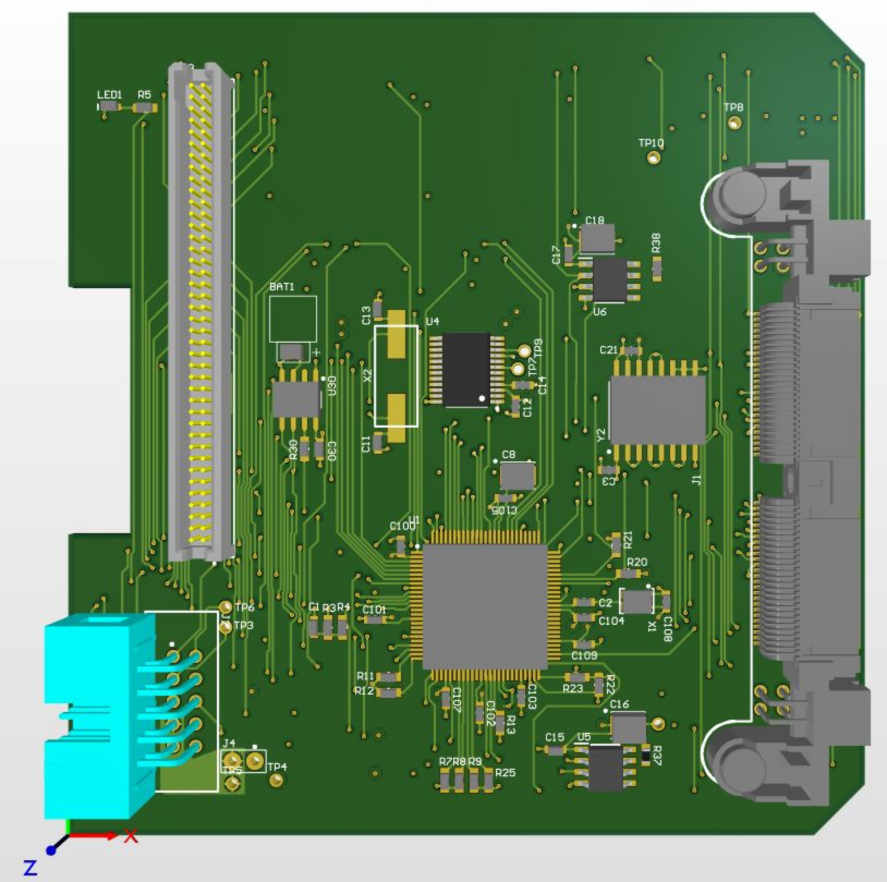


CDH - System Status: Layout

- CDH Board internal schematic review held and passed with minor changes
- Advanced Circuits 4-layer special Rules and Layer Stack inserted
  - Courtesy of Joe Buescher, a colleague working on AEPEX
- Initial layout completed, with reduced size to meet **KDR 1.1**
- New parts added and layout revised with advice and input from CANVAS' EE, Sebastian Wankmueller
- Routing first draft complete
  - Used MAXWELL advice with traces running directionally on signal layers
  - Larger Debug connector, paired with size reduction and number of connections caused significant, but solvable, issues

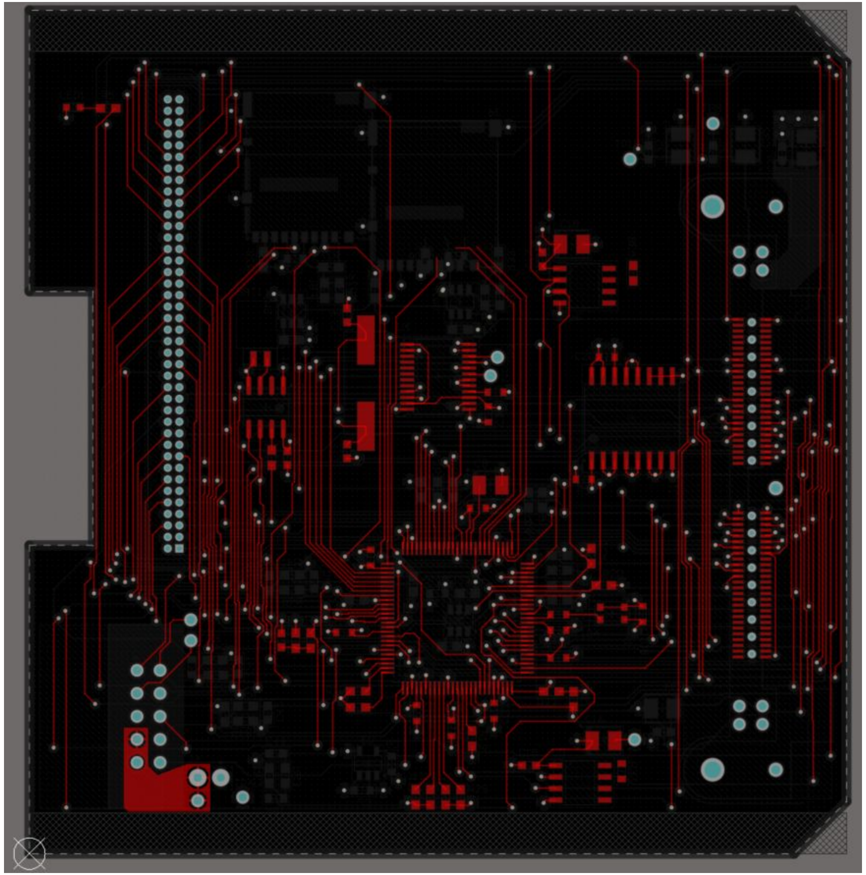
CDH - System Status: Layout



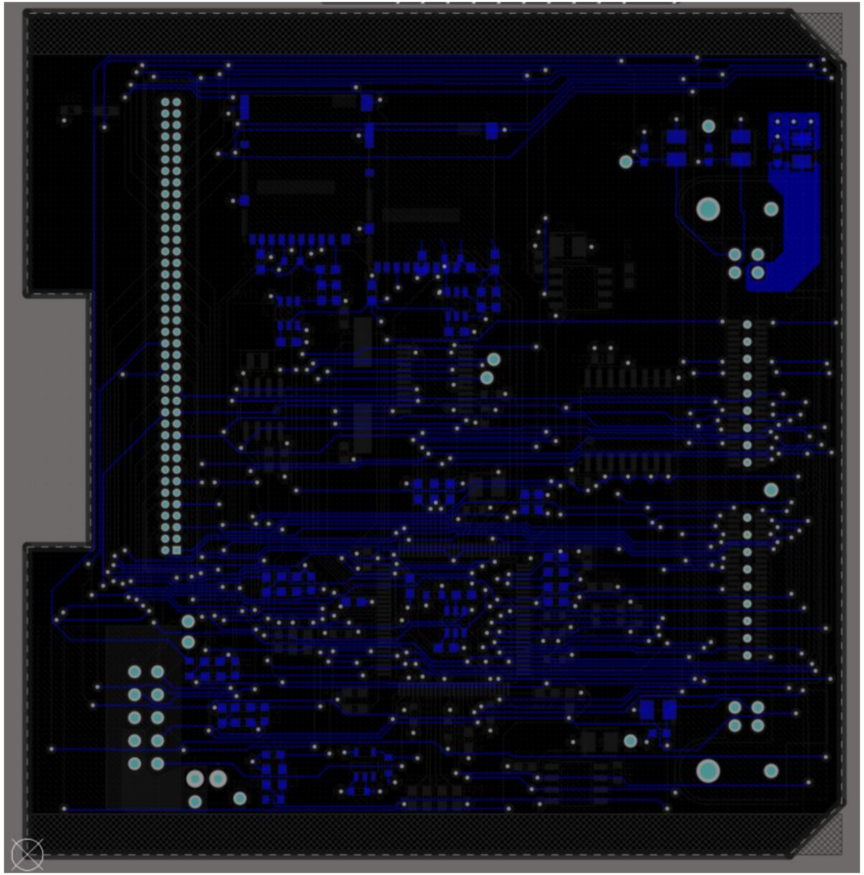


CDH - System Status: Layout

Top Layer



Bottom Layer



CDH - Next Steps

<u>Goal:</u> PCB designed completely and confidently, ready to procure, populate, test.

- Minor layout additions (1 Week)
- Redesign Documentation Updates (<1 Week)
- Layout Review (1 Week)
- 2nd Revision, if needed (2-4 Weeks)
- Prepare Validation and Verification Resources (testing plans/procedures)
  - GSE Board ready to use (see GSE section)
  - Unit test plans complete, procedures drafted

Board should then be ready for procurement, population, testing

CDH - Next Steps

Layout Additions

- Polygon GND pours
- Add Ferrite Bead to PIC microcontroller AVss
- Via-stitching of GND pours
- Check validity of power polygons
- Route differential pairs using Altium tool(s)
- Confirm via sizing
- Determine method for COSMO/CANVAS compatibility

Possible changes in next Revision:

- Extra routing space for Clock, Signal lines
- Reduce Debug signals/two smaller connectors

CDH - Next Steps

Unit Testing Plans/Procedures Development

- Continuity testing
- Power testing
- FSW upload testing
- Read/Write memory testing and memory capacity testing
- Digital signal testing (preferred GSE)
- Communication signal testing (preferred GSE)
  - Focus on new RS-422 translator
- Data integrity testing (requires GSE)
- EMI testing
  - Perform during constant read/write of SD cards → maximum current

Ground Station Equipment Board

Chadd for Max

GSE - Overview

- Ground Support Equipment Board
- Based on MAXWELL design
- Where data exchange occurs for ground testing
    - RS232, RS422, SPI, i^2C
- Translates communication protocols to USB
    - To be read by computer
- Allows for table top testing of CDH board
- Supplies ground power to CDH board
    - 3.3V

XACT RS422

XACT RS232

UHF RS232

PLD RS232

EPS RS232

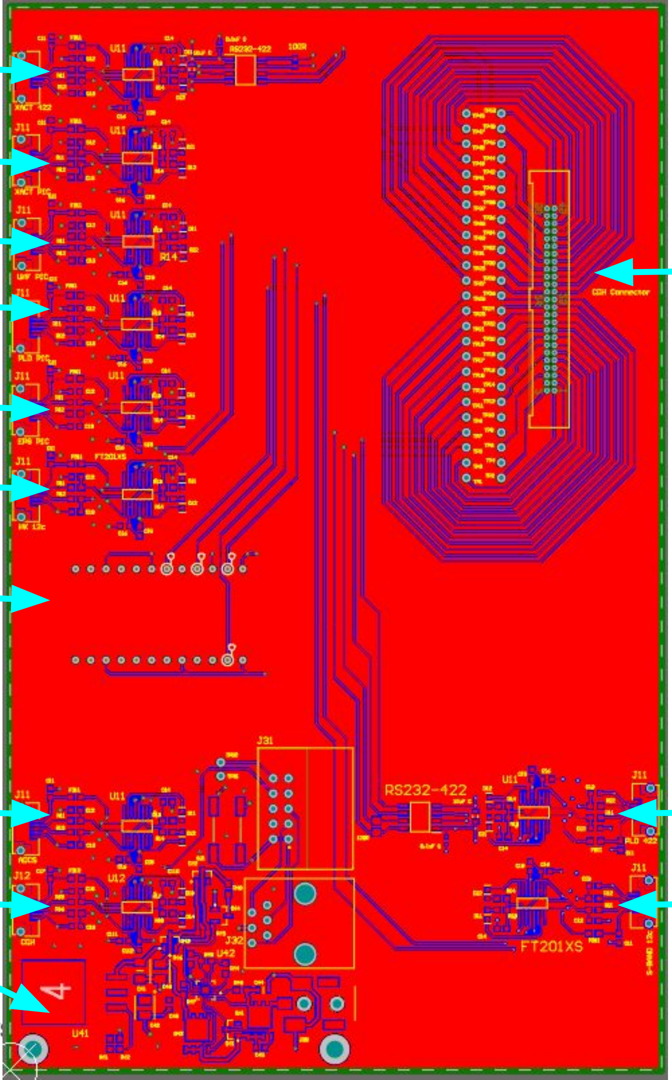
HK i2C

S-BAND SPI

ADCS RS232

CDH RS232

Power to CDH



CDH Debug

PLD RS422

S-BAND i2C

Signal List
XACT RS422
PLD RS422

XACT RS232
UHF RS232
PLD RS232
EPS RS232
ADCS RS232
CDH RS232

S-BAND i2C
HK i2C

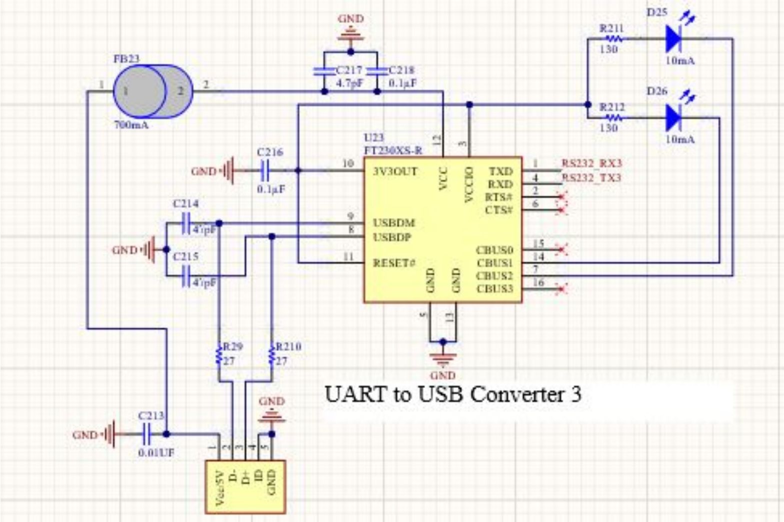
S-BAND SPI

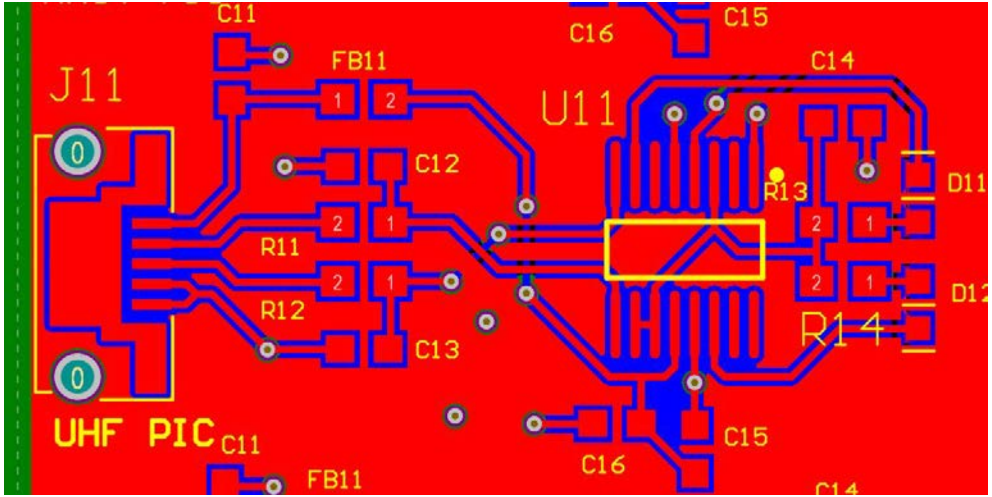
GSE - Key Requirements

Req.	Description	Reasoning
EGSE-8	All EGSE switches or buttons shall be clearly labeled	To avoid confusion when in use
EGSE-3	EGSE shall be capable of supporting functional testing of the satellite, including subsystem level, full functional testing, and full “day in the life” testing.	GSE Board must be able to support subsystem level testing of CDH - including interfaces to all other subsystems.
EGSE-11	EGSE shall be designed with fuses and diode protection to ensure that failures in ground support equipment or procedural mistakes will not damage CANVAS hardware or cause other hazardous conditions.	GSE Board failure/user-error could otherwise cause extreme damage to sensitive CDH microcontroller.

GSE - System Status

- Schematics and Layouts borrowed from MAXWELL
  - Successful heritage

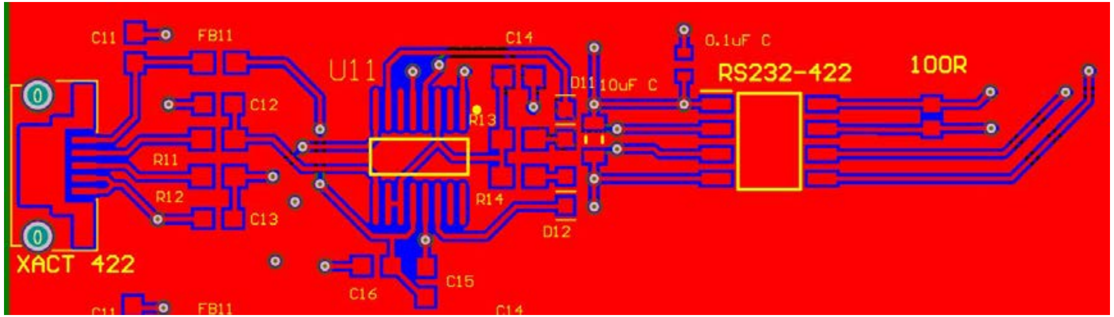


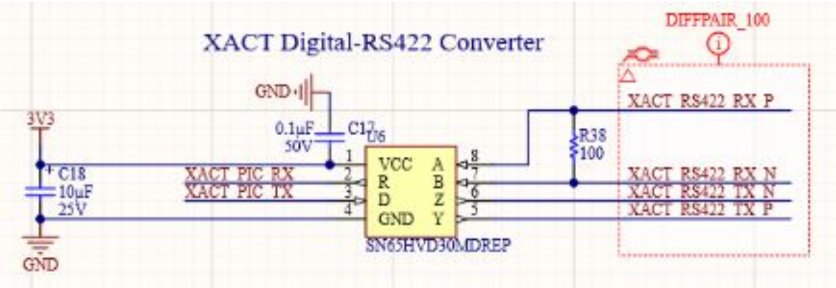


- i2C sections are identical except for the chip (FTDI201 instead of FTDI230)

GSE - System Status

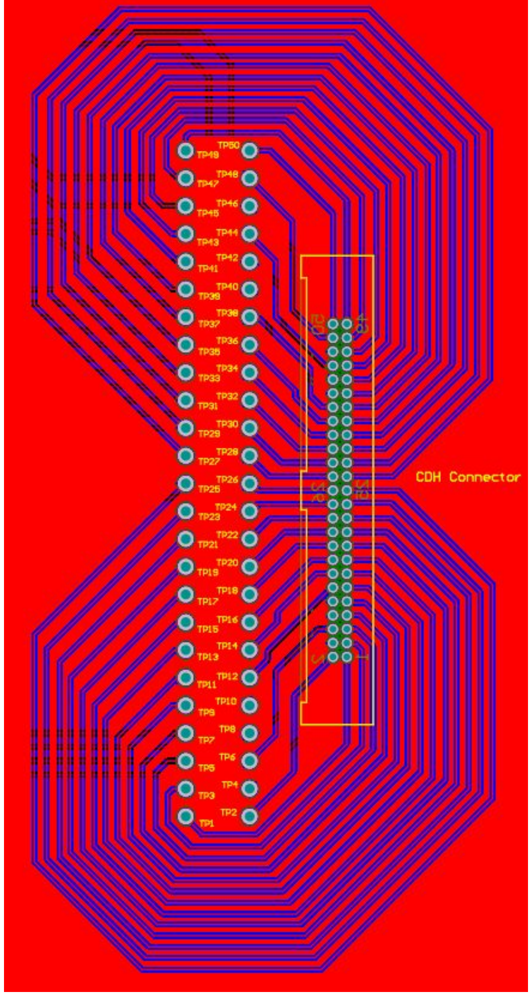
- For RS422, a converter from 232-422
  - Chosen by CDH
  - Used on GSE for consistency





GSE - System Status

- Similar layout to MAXWELL
- TP's laid out 0.1 in apart
  - To use std. Headers, ease of access



GSE - Next Steps

- Revise power section layout (1 week)
  - Currently fits MAXWELL’s board dimensions not CANVAS’
- Via stitch data lines (<1 week)
- Fix connection between Altium schematics and Layout (1 week)
- Create a BOM (<1 week)
- Procure and populate board (1 week)

Communication Subsystem

Kyle

Data Budget

FFT Frequency bins	67	bins
Time resolution (spectra/sec)	1	Hz
Spectral Matrix:		
Number of values: diagonal	5	values
Bit depth (diagonal)	8	bits
Number of values: off-diagonal	20	10 complex numbers
Bit depth (off-diagonal)	12	bits
Bits per spectral matrix	**280**	bits
Bits for time-tag	**64**	bits
Data production rate	**18824**	bits/sec

Packet Headers/day	148901	bits/day
Recording time per day	86400	sec
Total data produced per day	**193.899**	**MB/day**
Ground station coverage per day	15.16	min
(sec)	909.6	sec
Downlink rate	2.10E+06	bits/sec
Data downlink capability per day	**227.71**	**MB/day**
Margin	**14.848**	**%**

UHF Budget

CANVAS Data Budget (UHF Band)		
XACT minimal package	1944	bits
Frequency	0.01667	Hz
XACT quaternions	128	bits
Frequency	0.10	Hz
EPS Voltage and Current	8	bits
Frequency	0.01667	Hz
GPS position	300	bits
Frequency	0.01667	Hz
Thermal sensor readings	8	bits
Number of readings	5	readings
Frequency	0.01667	Hz
Data production rate	**51**	**bits/sec**
Packet Headers/day	432	bits
Recording time per day	86400	sec
Total data produced per day	**0.5253**	**MB/day**
Ground station coverage per day	15.16	min
(sec)	910	sec
Downlink rate	9600	bits/sec
Data downlink capability per day	**1.041**	**MB/day**
Margin	**49.53**	**%**
Redundancy?		

Comms Subsystem Status

S-Band

- Payload data downlink
- 194 MB/day
  - 2.1 Mbps data rate needed for 20° elevation mask

UHF

- Telemetry, housekeeping, beacon downlink
- Command uplink
- 0.52 MB/day downlink
  - Data rate: 9.6 kbps

Comms Key Requirements

Req.	Description	Reasoning
Comm-4	The subsystem shall downlink payload data in S-band frequency band	Payload data must be transmitted to the LASP ground station
Comm-5	The subsystem shall be capable of receiving uplink commands and downlinking telemetry and system status in the UHF frequency band	S/C must accept commands and transmit beacon from the LASP ground station

COMMs - Radios

UHF: Astrodev Li-2

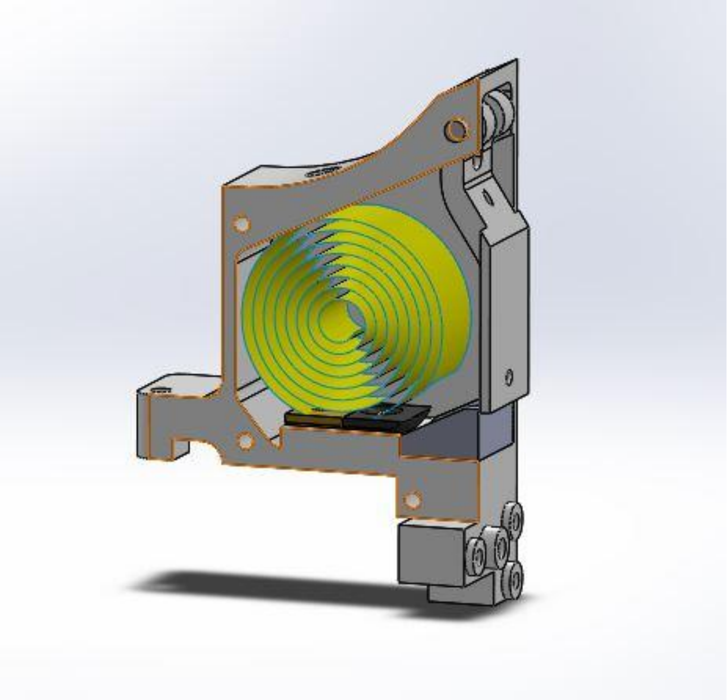
- Will fly on MAXWELL
- LASP has lots of experience
  - Mixed on-orbit performance
  - Possible ConOps planning necessary

S-Band: Clyde Space HSTX

- Planned use in INSPIRESat - 1&2
- Forward correction encoding helps with BER (coding gain)
- Consistent with COSMO

COMMs - Antennas

UHF: LASP tape measure antenna



S-band: Clyde Space patch antenna

Link Budget

CANVAS S-Band Link @ 500 km				
Data Rate (Mbps)	1.27	2.1	1.27	2.1
Elevation (deg)	10	20	10	20
G/T (dB)	*14.1*	*14.1*	*0*	*0*
Link Margin (dB)	**6.6**	**7**	**-7.2**	**-6.8**

CANVAS UHF Link @ 500 km				
Uplink/Downlink	*Up*	*Up*	*Down*	*Down*
Tx/Rx Power (W)	*250*	*250*	*2*	*1*
Data Rate (kbps)	9.6	9.6	9.6	9.6
Elevation (deg)	10	20	10	20
Link Margin	**27.3**	**30.3**	**6.9**	**6.9**

- AMSAT / IARU Standard Link Budget System
- Data rates used:
  - S-Band: 2.1 Mbps*
  - UHF: 9.6 kbps
- Evaluated at 500 km altitude
- Ground Station S-band values unconfirmed by LASP
  - Somewhere between 0.0 - 14.1 dB G/T

COMM-3	The subsystem shall have a minimum link margin of +6 dB on uplink and downlink at 20° degree elevation mask

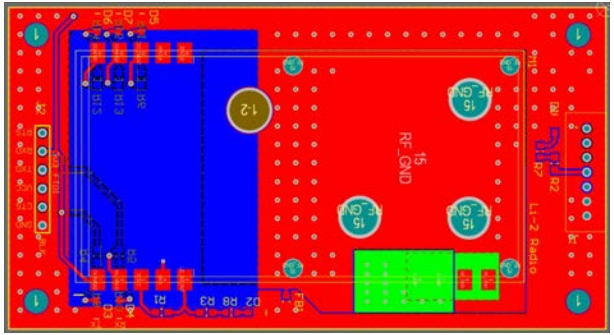
COMMs - Next Steps

- Hardware purchased, procedures initialized, interfacing well defined, pointing requirements well understood
- To be Completed:
  - Purchase and build of test components (I.e. MAXWELL UHF PCB)
  - UHF antenna part order, build, and test
  - Procedures to be refined and approved by management
  - Component testing and interfacing
  - HYDRA commanding maturation with FSW

CU Boulder Aerospace Department
COSMO
University of Colorado
Boulder, Colorado

COSMO Procedure Li-2 Radio Configuration Test Document Form No XX.XX

Approvers List	
Prepared By	COSMO Comms Engineer
Approved By	COSMO Project Manager
Approved By	COSMO Systems Engineer



COMMs - Next Steps: Proposed UHF Tests

- **PCB Build and Integration**
  - PCB backplane from MAXWELL heritage
  - Self-populate and test backplane PCB
  - Receive and test (power, resistance) professionally assembled PCB backplane
  - Attach (solder) professionally assembled backplane to UHF radio
- **Configuration Test**
  - Radio hardwired to PC running configuration software
  - Check pre-configured parameters and change them if necessary
  - Confirms radio powers on and can send/receive serial commands
- **Hardwired Commanding Test**
  - Hardwired Rx and Tx to PCs running HYDRA
  - Rx “commands” from PC, Tx “commands” to PC
  - Confirms radio is able to transmit and receive, HYDRA works as planned
- **Hardwired Commanding Test with CDH**
  - Hardwired Rx and Tx to PCs running HYDRA
  - CDH and HYDRA incorporated
  - Rx commands from PC, Tx commands to PC
  - Confirms radio is able to transmit and receive actual commands, HYDRA works as planned
- **RF Test**
  - Full verification of Comms KDR Comm-5
  - Test to understand data rate and verify RF transmission and reception of data
  - Incorporates HYDRA commanding and SANT antenna

COMMs - Next Steps: Proposed S-Band Tests

- **Hardwired Commanding Test with CDH**
  - Hardwired Tx to PCs running HYDRA
  - CDH and HYDRA incorporated
  - Change modes via I2C and check changes
  - Transfer “data” via SPI
  - Tx data confirmed by reading buffer over/underrun registers via I2C
  - Confirms radio is able to transmit data, HYDRA works as planned
- **RF Test**
  - Full verification of Comms KDR Comm-4
  - Test to understand data rate, verify buffer timing is correct, and verify RF transmission
  - Incorporates HYDRA commanding

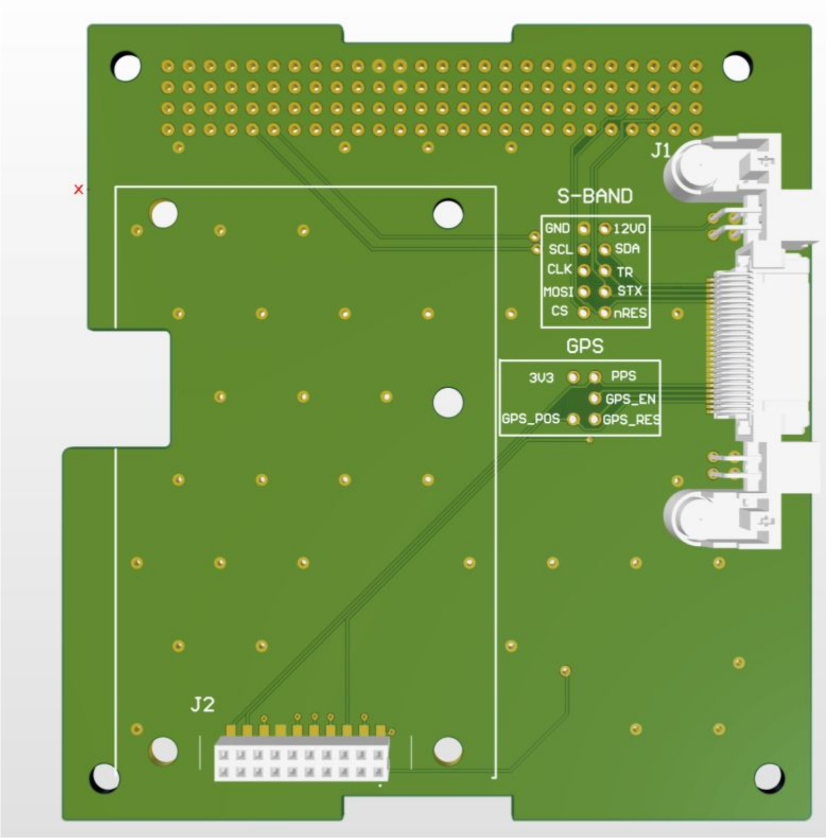
Leverage test plans from INSPIRESAT

S-Band and GPS Daughter Board

Jett

S-Band Daughter Board - Overview

- Board to connect the ClydeSpace HSTX-01-00073 S-Band Transmitter to the backplane.
- Dimensions match the transmitter
- GPS adapter on CANVAS
- Header pins for signal testing
- Fits in board stack
  - No rails due to connector interference.
  - Notch in walls of structure to fit DB and transmitter

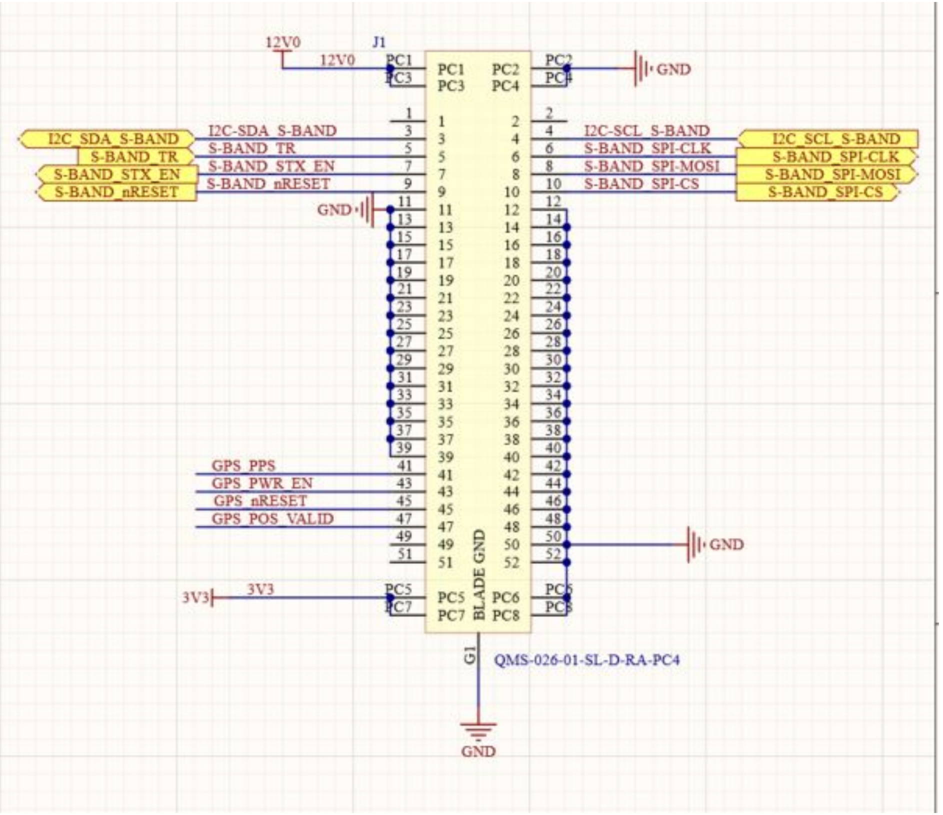


S-Band Daughter Board - System Status

- Schematics and Layout finalized
    - 2 Layer special from Advanced Circuits used for layer stack.
- GPS connector added
- Routing complete
- Rules verified
- Gerber check needed

S-Band Daughter Board - System Status

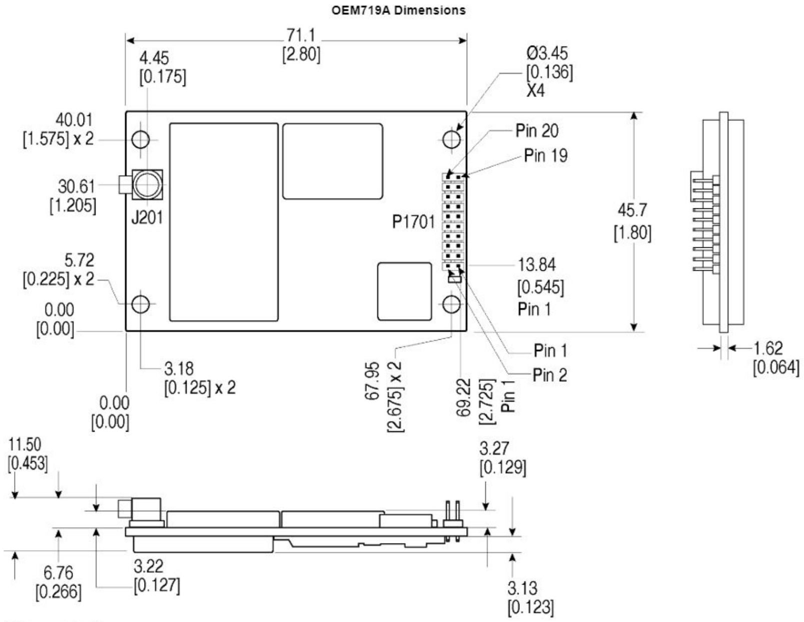
- Power Pins utilized for 12V and 3.3V inputs.
- GPS and S-BAND output to PC4 connector



S-Band Daughter Board - GPS

- OEM 719A selected
  - Right angle MCX Jack
- Standoffs required between GPS and Daughter Board
- Interface connector is TLE-110-01-G-DV-A-TR.
  - 2mm pitch
  - (-55℃ to 125℃)

Dimensions are in millimetres [inches].



Notes: 719A
Dimensions are in millimetres [inches].
Connectors:
(a) J201 MCX jack receptacle, right angle (Samtec P/N MCX-J-P-H-RA-SMI or equivalent)
(b) P1701 2x10 header, 2 mm pitch (Samtec P/N TMM-110-03-G-D)

Mechanical specifications for OEM719A

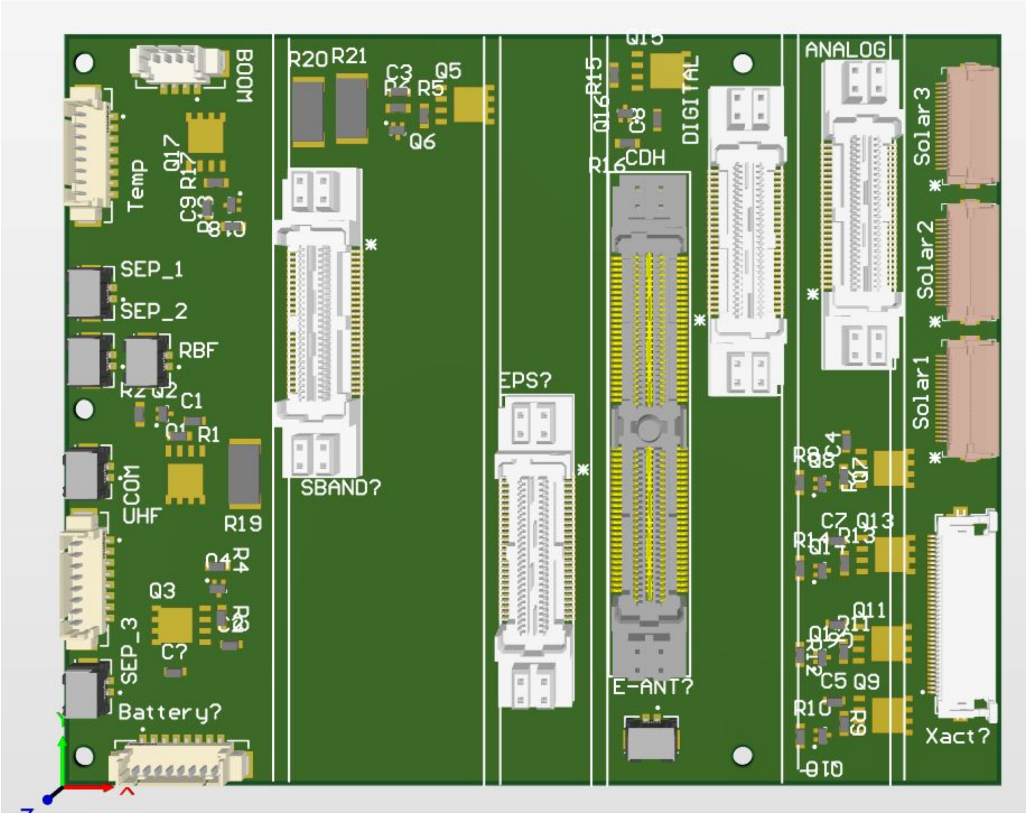
S-Band Daughter Board - Next Steps

- Prepare Gerber files(2 weeks)
  - Get approved by Advanced Circuits
  - Procure board
- Procure Board
- Populate Board(2 Days)
- Continuity testing using test points on the daughter board(1 month)
  - Need Oscilloscope/ Multimeter

Backplane and Wiring

Jett

Backplane and Wiring - Overview



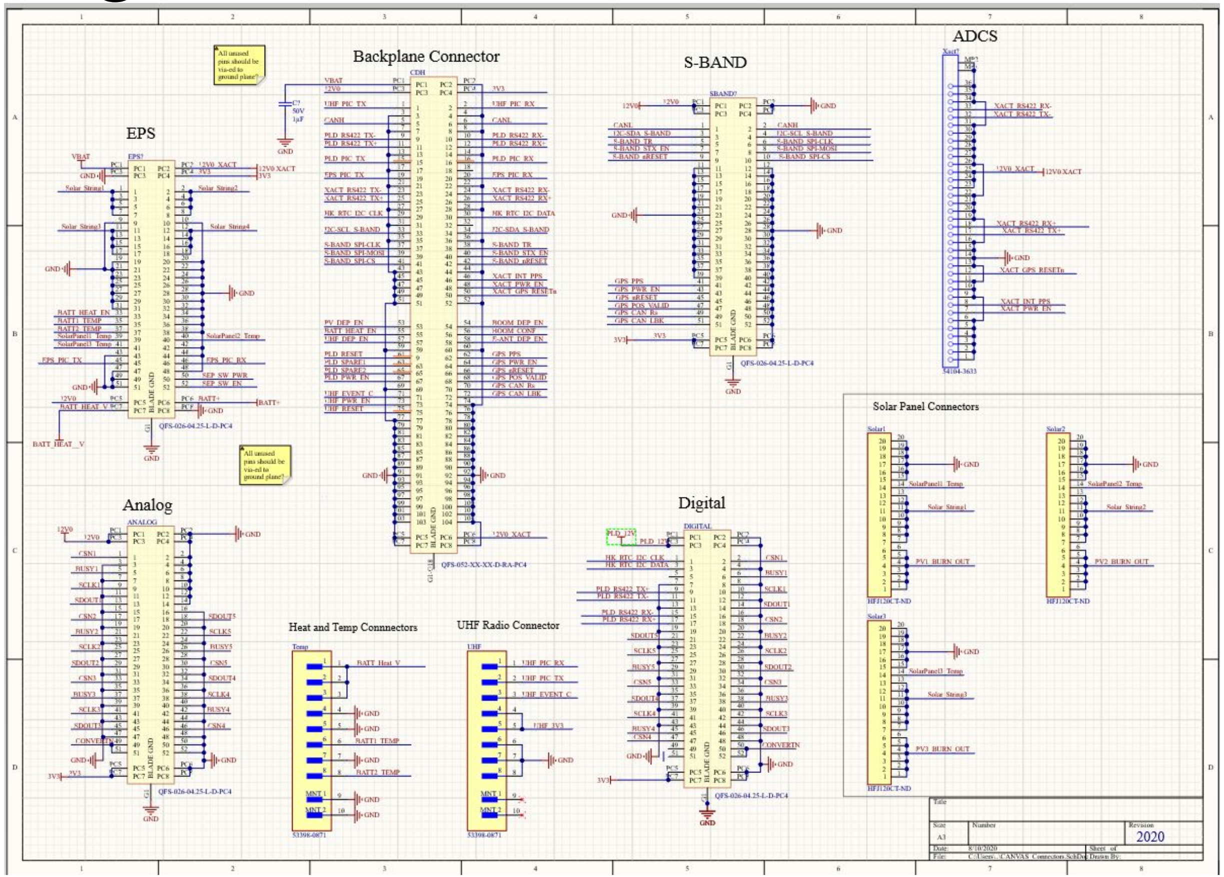
- The backplane connects most of the electronics in the spacecraft
- The primary boards(S-BAND DB, CDH, EPS, Analog and Digital) are included in a board stack
- Dimensions are 105.2x84.3mm
- Contains power enable and burnout circuitry
  - Enable:
    - UHF, Payload
  - Burnout:
    - Solar Panels, Comms, Boom, E-Field Antenna

Backplane and Wiring - Key Requirements

Req.	Description	Reasoning
EPS-11	The subsystem shall adhere to all Electrical System Design and Inhibits outlined by NRCSD	We cannot launch if we do not meet the requirements set out in the NRCSD IDD
EPS-11.4	The subsystem design shall incorporate a minimum of three (3) independent inhibit switches "actuated by physical deployment switches as shown in Figure 4.2-1.	This is to assure the spacecraft doesn’t power up before deployment
EPS-11.6	The RBF / ABF feature shall preclude any power from any source operating any satellite functions except for pre-integration battery charging	This is to assure the spacecraft is not powered during integration and ground handling

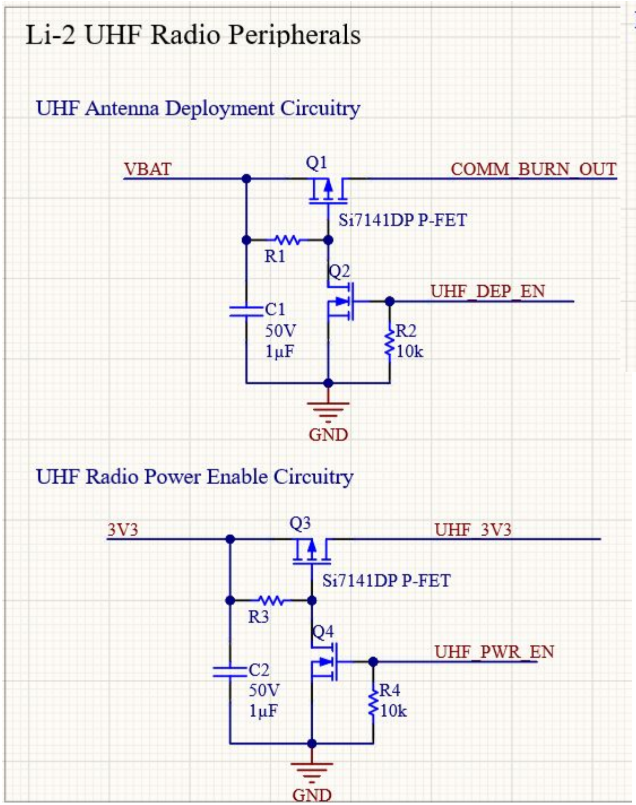
Backplane and Wiring - Connectors

- Same connector selection as COSMO
- Analog and Digital Boards added to cardstack
  - Most connections between boards
  - PLD connections to Digital Board

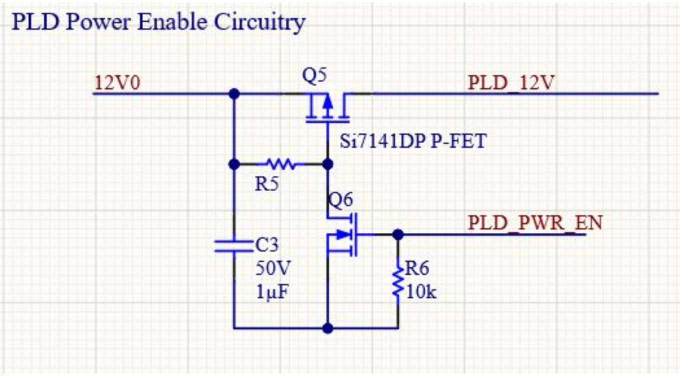


Backplane and Wiring - Connectors

- Based on MAXWELL heritage
- Uses battery voltage(14.8V) for burnout circuits
- All burnouts have same voltage and configuration as UHF Deployment circuitry on the right
- Additional Burnout circuitry added for Boom and E-Field Antenna.

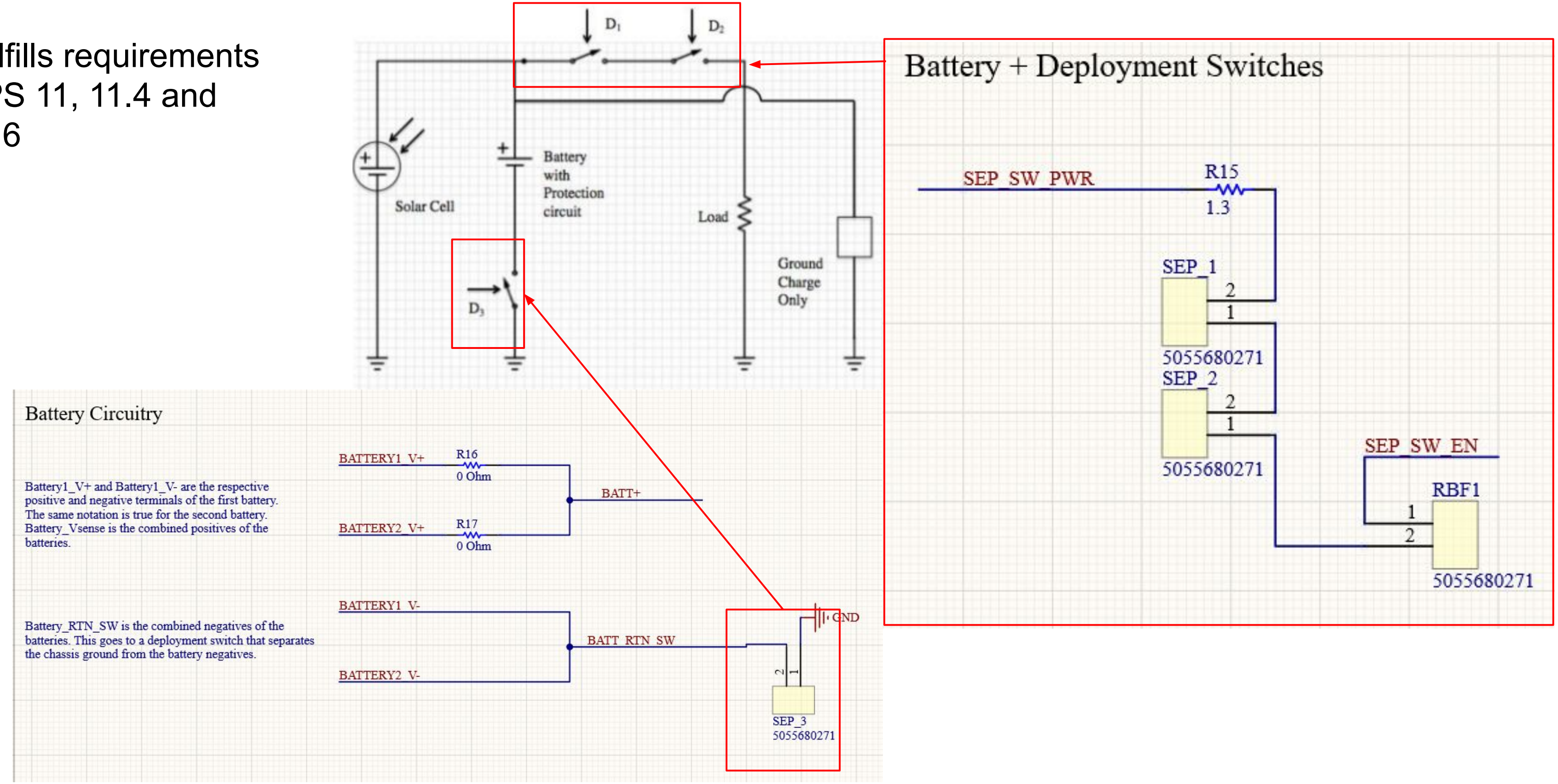


UHF Enable Circuitry



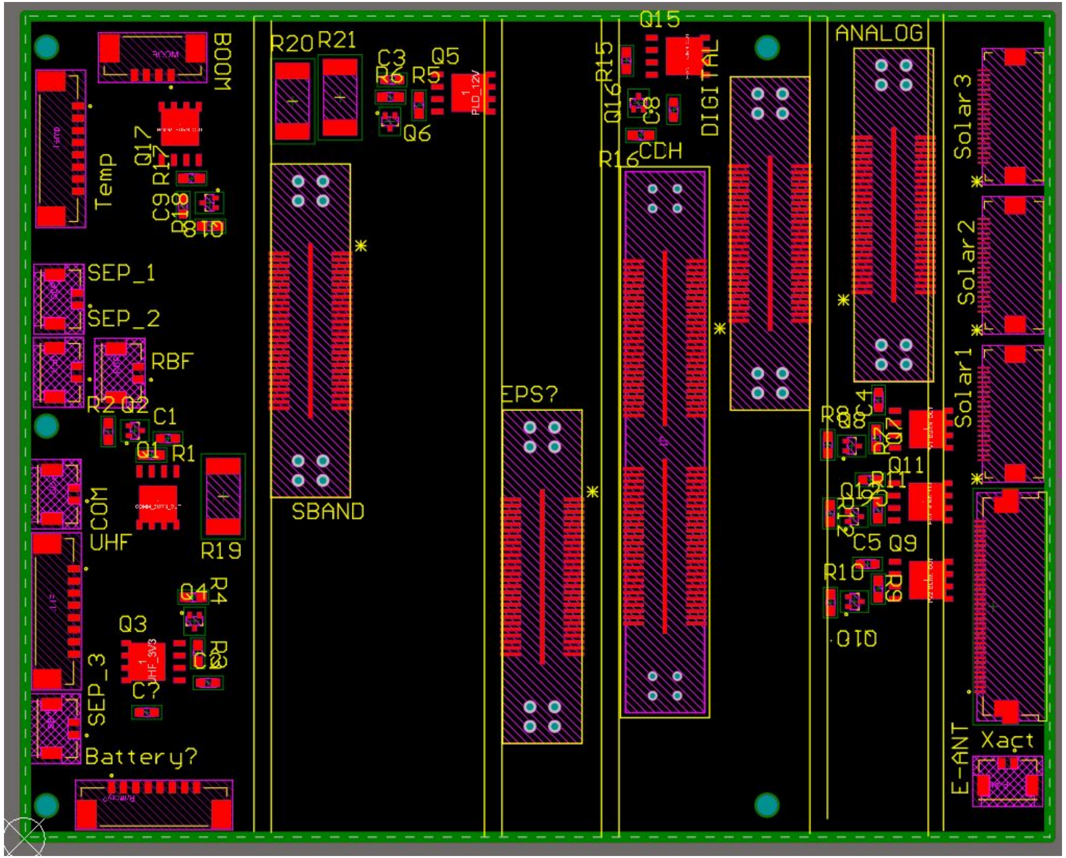
Backplane and Wiring - Connectors

- Fulfills requirements EPS 11, 11.4 and 11.6



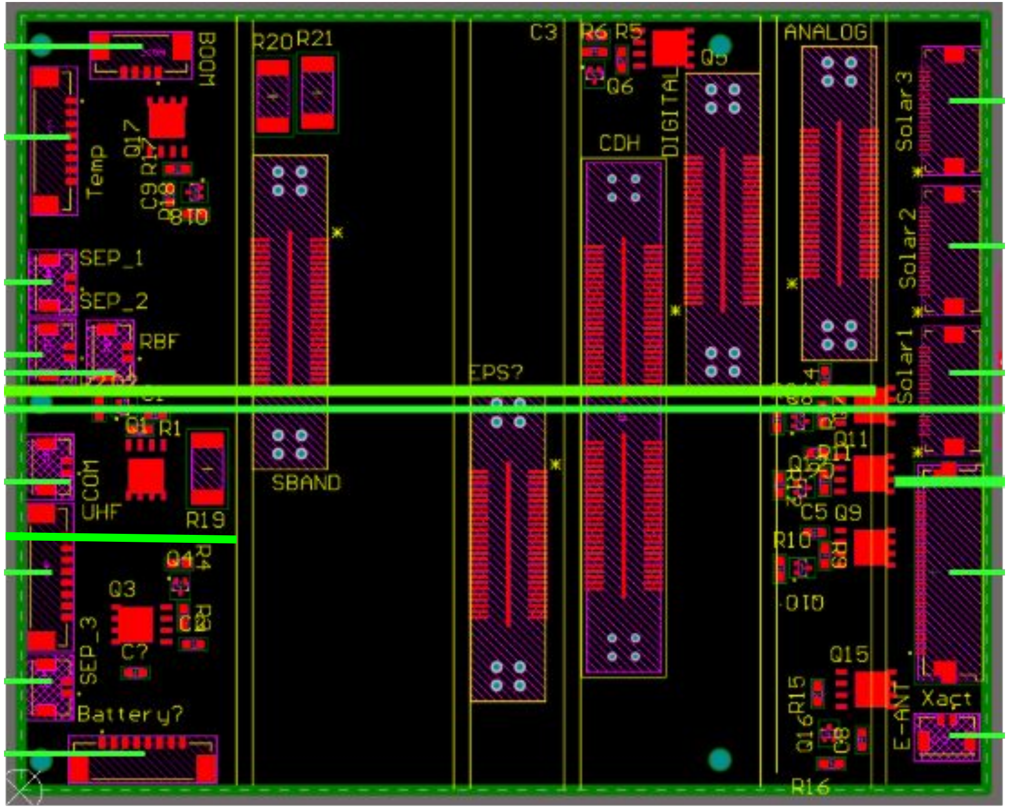
Backplane and Wiring - Layout

- Layer stack based on Advanced Circuits 4 layer special
- Connector Placement done
  - EPS distanced from Analog board to avoid EMI
- Needs to be routed
- GND plane should be dedicated to DGND
- Rules already implemented
  - Design Rule Check needed
- Auto route was 96.3% complete



Backplane and Wiring - Layout

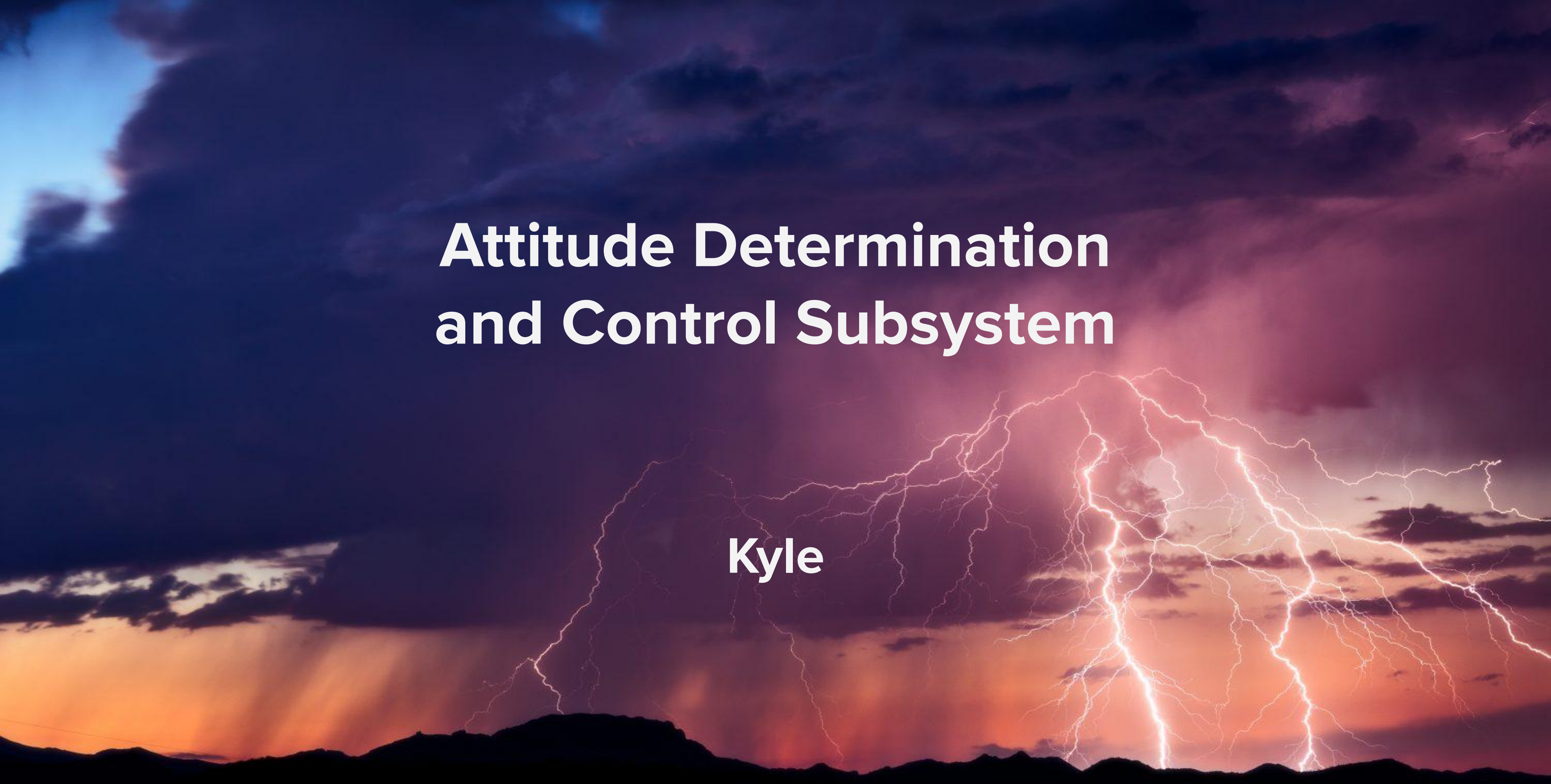
- Notch added in cardstack, opposite backplane connector for external wire routing
- Notch is necessary for B-Field Science and suns sensors
    - Shown by green lines across board
    - Connect to Analog board



Green shows external wires that must be routed

5 Minute Break

Return at 4:05pm



Attitude Determination and Control Subsystem

Kyle

ADCS - Overview

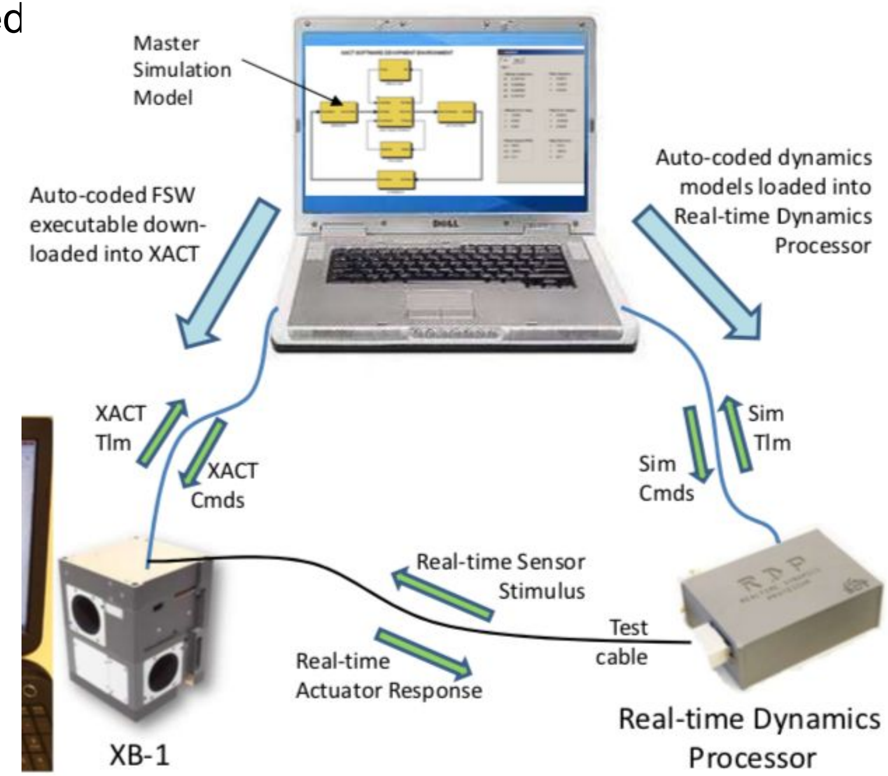
- COTS XACT package from Blue Canyon Technologies
    - 3 Reaction wheels
    - 3 orthogonal torque rods
    - Coarse sun sensor
    - Star tracker
    - Internal magnetometer
    - IMU
- 1 EDU and RDP shared between COSMO and CANVAS for on-orbit dynamic simulations
    - Will be able to reprogram for CANVAS mission as future development is completed
    - “Rev 2” ICD Addendum has been sent to BCT: 7/17/20

ADCS Key Requirements

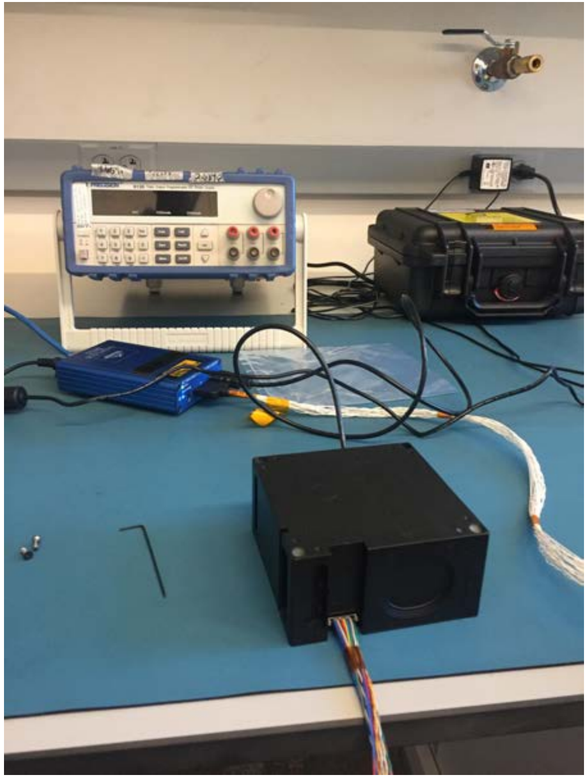
Req.	Description	Reasoning
ADC-1	CANVAS shall use the Blue Canyon Technologies XACT-15	BCT XACT already purchased.
ADC-3	Subsystem shall be capable of determining its attitude within an accuracy of 1 degree	VLF wave component direction shall be known within 1 degree
ADC-5	The subsystem shall provide attitude control for all modes defined in the CONOPs	CANVAS shall be capable of charging its batteries, communicating with the ground station and downlinking data.

ADCS - System Status

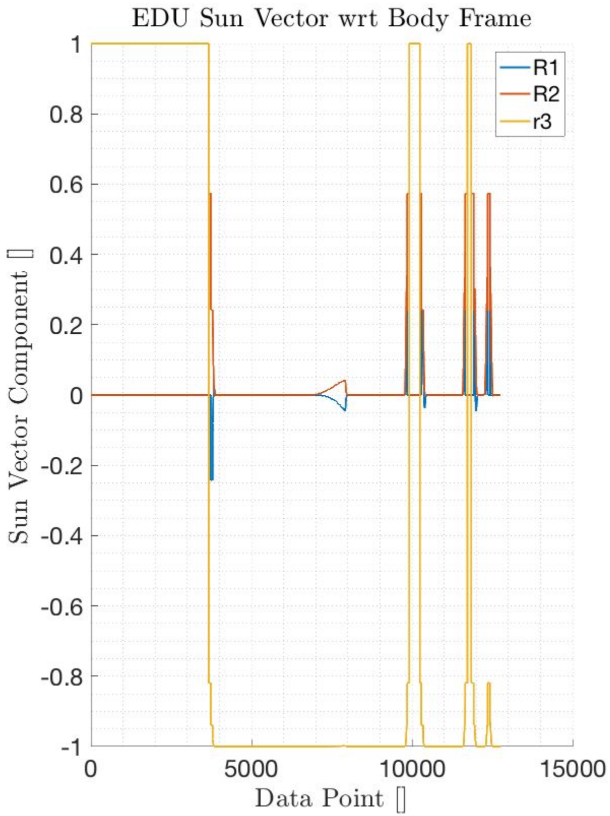
- Hardware-in-the-Loop testing conducted using RDP/COSMOS interface
- COSMOS provides command sending interface to check sent and received commands, telemetry packet counts, and raw data plotting
- Host machine sends simulated commands, and the RDP provides sensor stimulus to EDU
  - EDU responds with fabricated telemetry that is propagated by RDP simulations

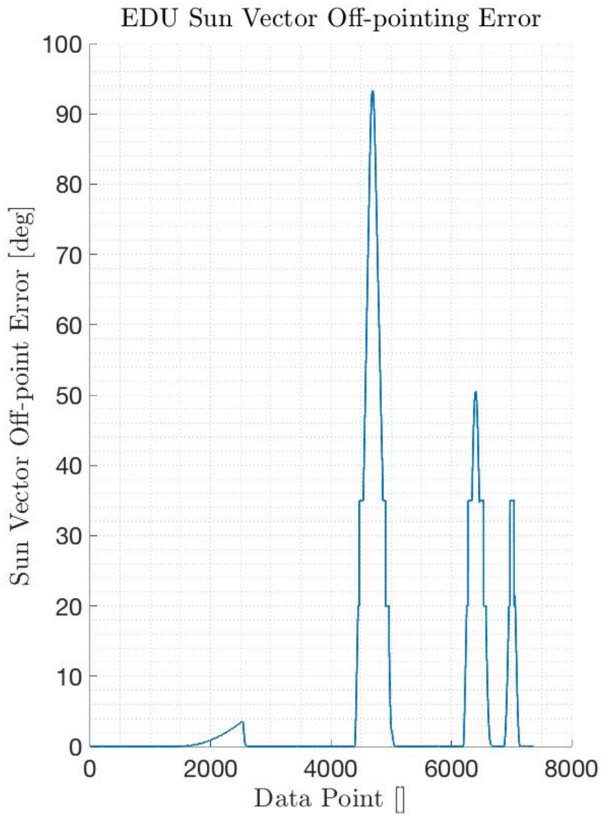


ADCS - System Status

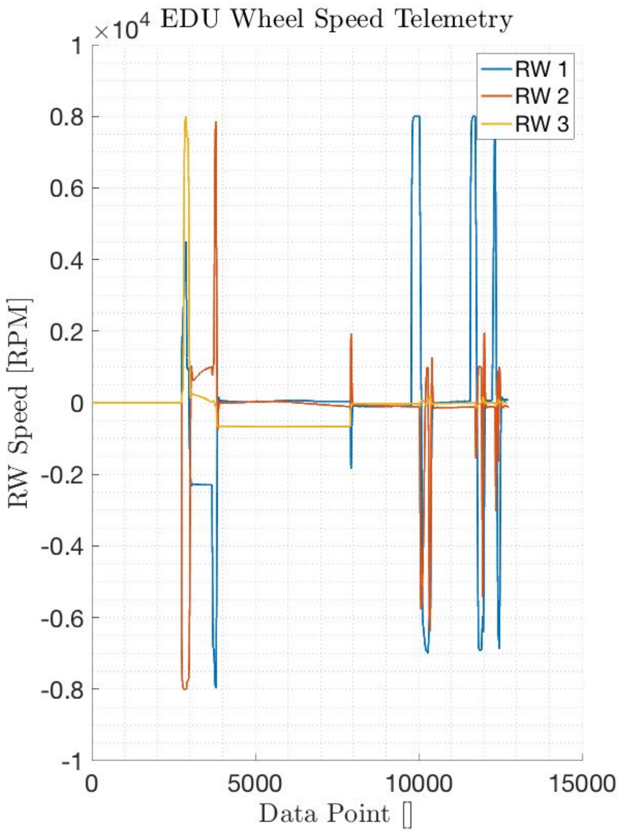


ADCS

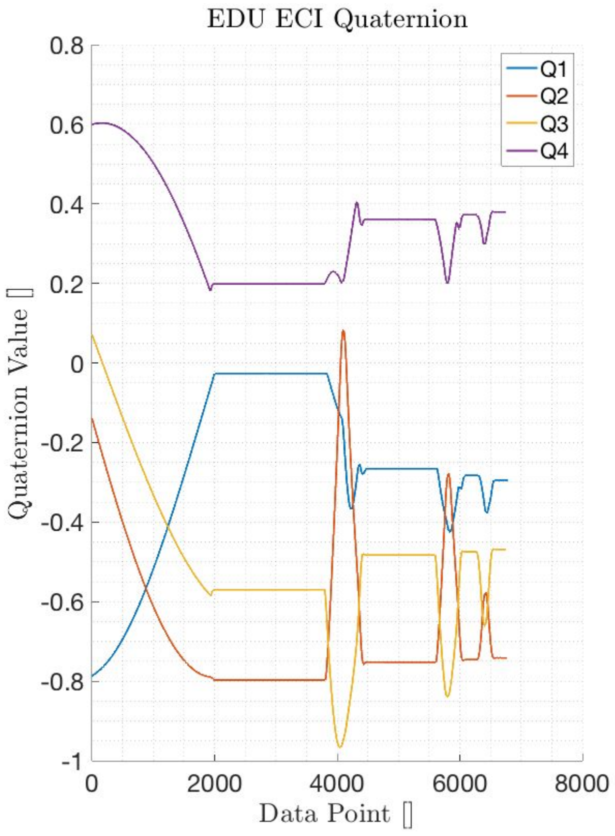

EDU Sun Vector wrt Body Frame
R1
R2
r3
Sun Vector Component []
Data Point []
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
5000
10000
15000


EDU Sun Vector Off-pointing Error
Sun Vector Off-point Error [deg]
Data Point []
100
90
80
70
60
50
40
30
20
10
0
0
2000
4000
6000
8000

ADCS



EDU Wheel Speed Telemetry
×10^4
RW 1
RW 2
RW 3
RW Speed [RPM]
Data Point []
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
5000
10000
15000



EDU ECI Quaternion
Q1
Q2
Q3
Q4
Quaternion Value []
Data Point []
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
2000
4000
6000
8000

ADCS - Next Steps

- Test assumptions to determine XACT behavior
  - Compare XACT EDU simulations with STK behavior
    - Sun-Pointing aligned/constrained
    - WMM aligned/constrained
    - LASP targeting
    - Attitude switching
- Run Monte-Carlo sims given a normally distributed 10 ± 2 deg/s tip-off body rate for the stowed configuration
  - Needs to reduce body rate to 0.5 deg/s for deployment mode
- MC sims for pointing accuracy during downlinking
  - MC sims will also help determine bus-boom interactions during mode switching
- Continue developing test plans for XACT arrival possibly in October
  - Investigate air-board testing for single axis rotations
  - Investigate testing methods for glint-free mitigation

Flight Software

Chadd for Lea

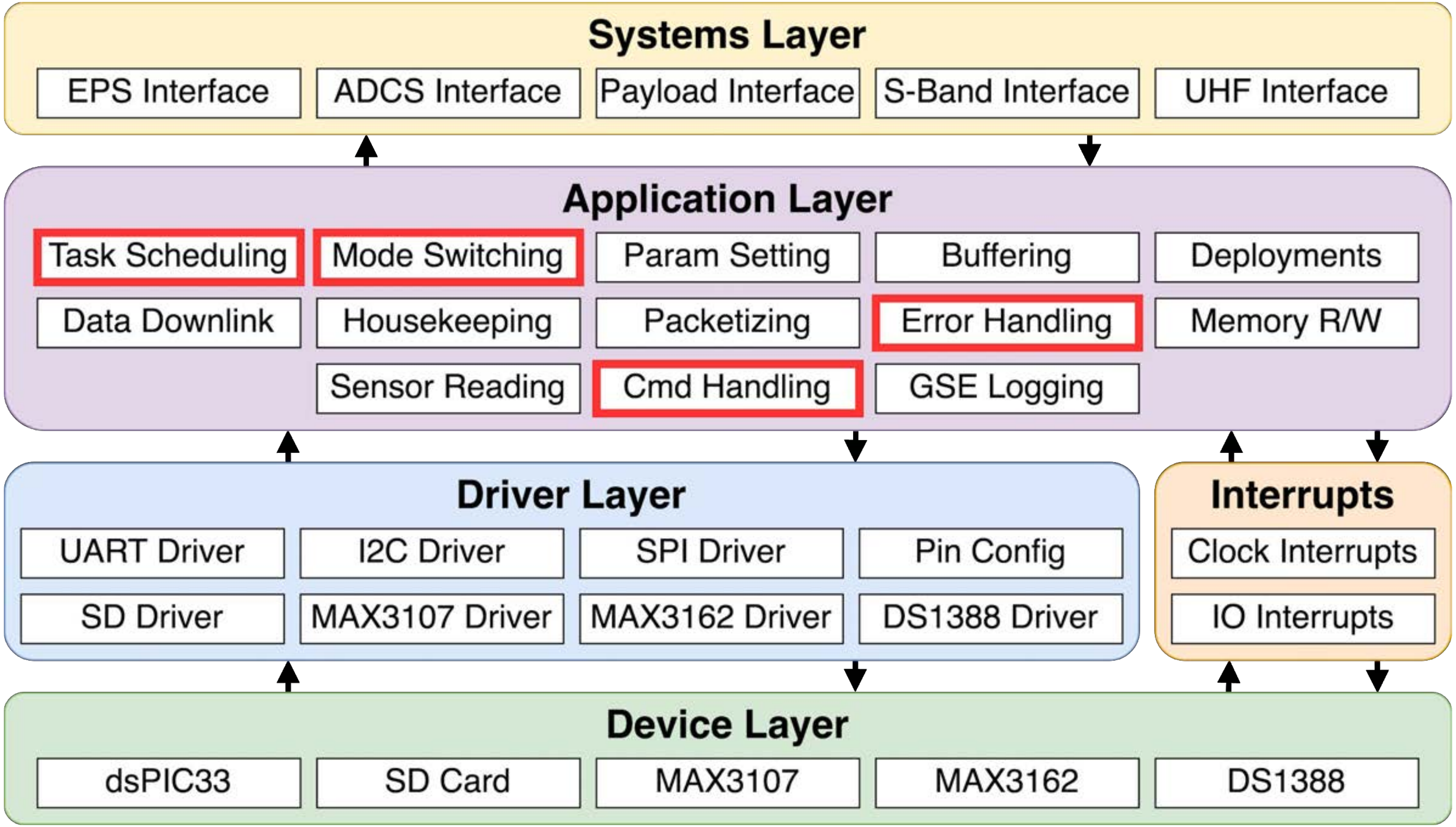
FSW - Overview

- Using MAXWELL heritage FSW for CDH and EPS
- No OS for multithreading - tasks are called sequentially
- Handles spacecraft modes, housekeeping, command routing, data downlink
- Packages data and acknowledges messages across interfaces
- Development with Microchips's MPLab IDE and 16-bit compiler

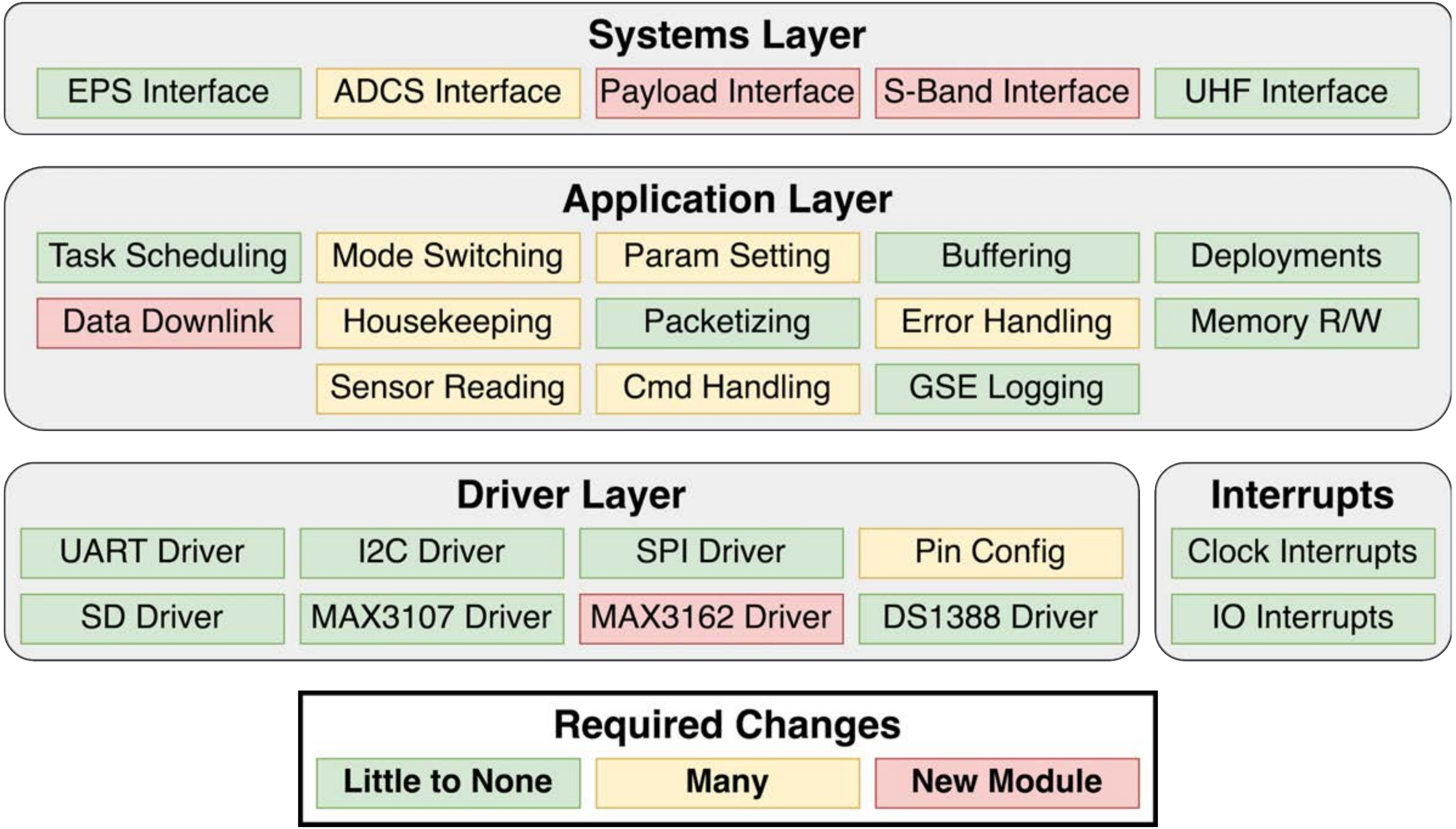
FSW - Key Requirements

Req.	Description	Reasoning
FSW-5	The software shall autonomously manage a set of spacecraft modes and dictate behavior in each mode defined in the CONOPs	This is required so that the the spacecraft can operate autonomously.
FSW-7	The software shall authenticate, process, and route ground commands to the appropriate subsystem.	This assures the other spacecraft subsystems receive commands from the ground.
FSW-15	The software shall support error handling.	This is to assist with recovering from SEEs and general subsystem errors.

FSW - CDH Software Architecture



FSW - CDH Software Heritage

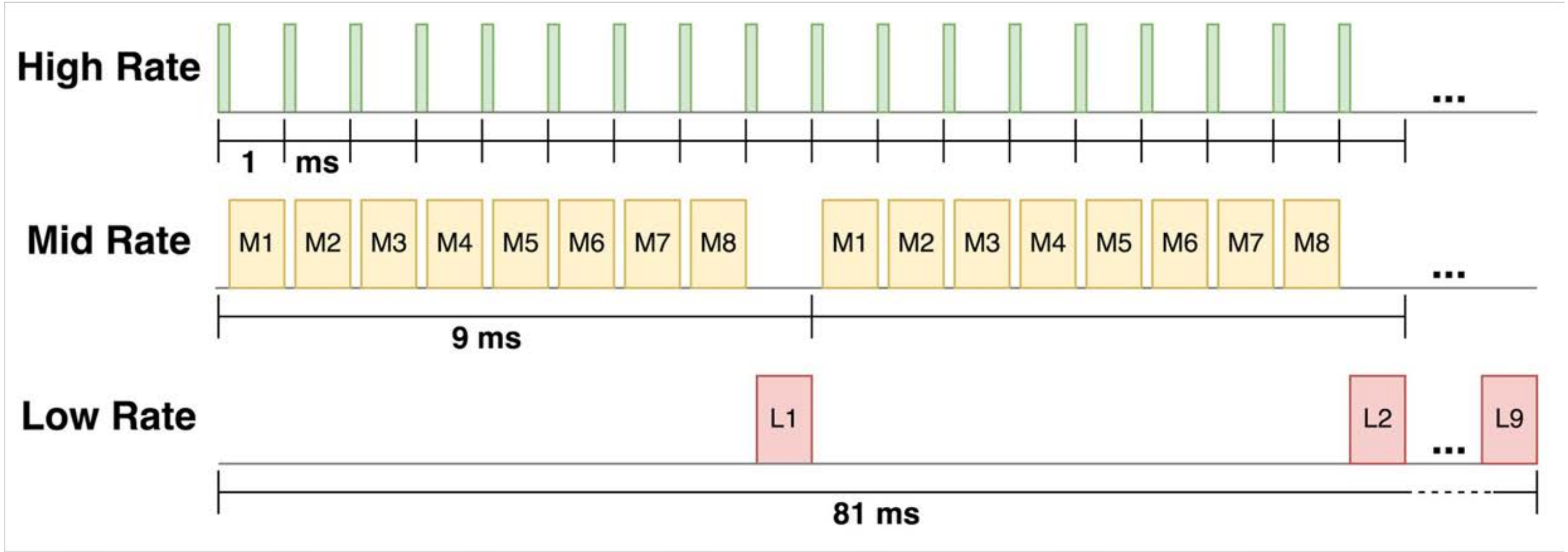


FSW - CDH Task Scheduler

High Rate Tasks
High priority tasks
(watchdog reset)

Mid Rate Tasks
Time sensitive tasks
(interfaces, spacecraft operations)

Low Rate Tasks
Slow or multi-second tasks
(deployments, spacecraft monitoring)



FSW - CDH Tasks

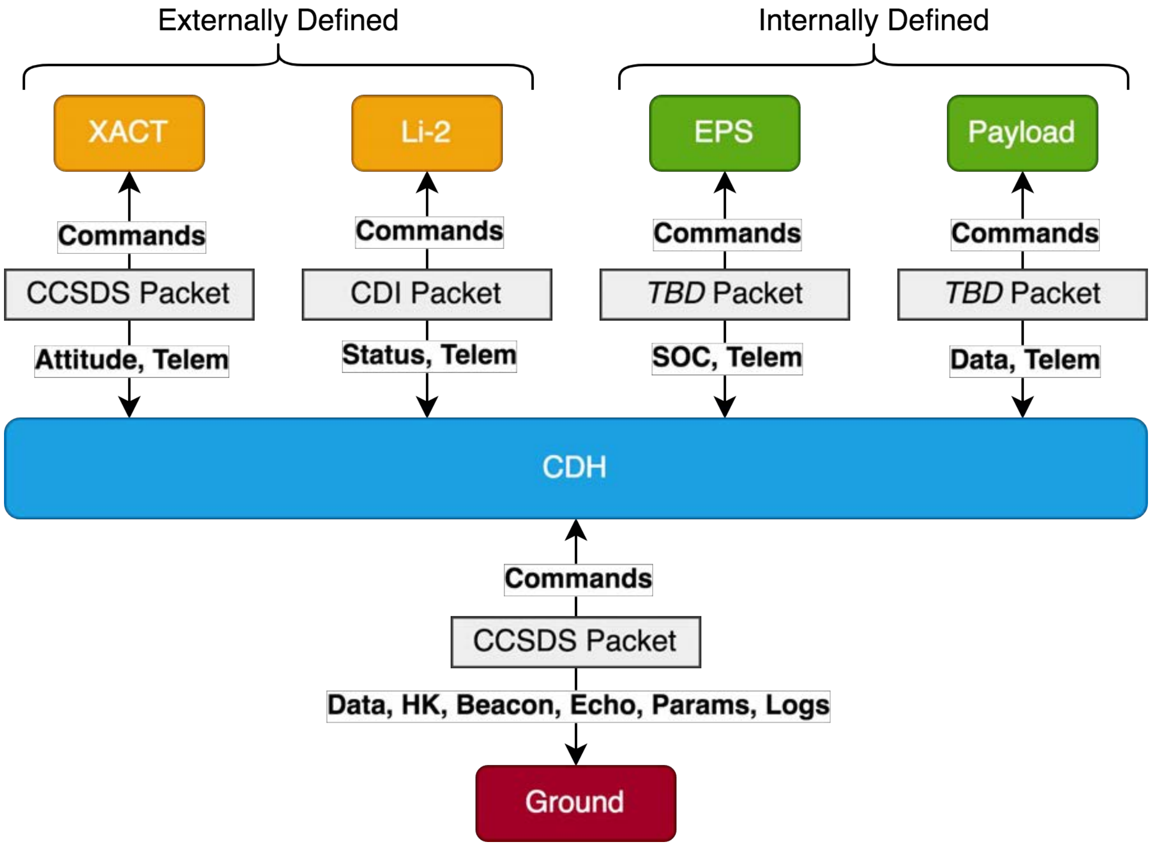
Mid Rate Tasks
<u>Interfaces:</u> 1. EPS 2. ADCS (MinXSS) 3. payload <u>Spacecraft Operation</u> 4. mode switching 5. data downlink 6. command handling 7. error handling 8. write table parameters

Low Rate Tasks
<u>Deployments</u> 1. antenna 2. solar panels <u>Spacecraft Monitoring</u> 3. read sensors 4. housekeeping 5. battery heater 6. check ground contact 7. read memory 8. check radio configuration

Status

- S-Band (HSTX) interface is defined and outlined
- ADCS (XACT) interface is defined and outlined
- ADCS task design in progress
- Spacecraft mode and switching limits in progress

FSW - Packet Types



Status

- Started definition of XACT data values, packets, and commands from ICD
- Li-2 heritage code includes CDI packet and opcode definitions
- Selected initial downlink opcodes

Note: The HSTX is purely a transmitter, so packetized data is downlinked as is. Commands and telemetry are transmitted over I2C.

FSW - Development Preparation

- Created coding standards, github repositories, and Doxygen documentation
- Documented environment setup, git access, and links to documentation
- Notes and task tracking for each file

Style Guidelines	- 4 space indentation - spaces around operators - parentheses around conditions - curly brackets for all conditionals
Naming Convention	- functions and variables are lowercase with underscores - pins and defines are all uppercase - no difficult abbreviations

Code Comments	- Doxygen style comments:
	    - File brief, author, date, and links
	    - Function brief, inputs, returns
	- Add assignee to TODO comments

FSW - V&V

Req	Short Description	Test	Method
FSW-5	Mode switching and behavior	Demonstrate mode switching and rejection of invalid mode transitions. Demonstrate that tasks execute as expected in each mode. Demonstrate sending valid commands and data across interfaces.	Unit test mode switching algorithm. Log messages and timing results over GSE during test.
FSW-7	Command handling	Demonstrate processing of commands. Demonstrate that corresponding handlers execute and behave as designed.	Unit test cmd processing and routing. Log messages and counters over GSE during test.
FSW-15	Error handling	Demonstrate recovery from invalid modes, commands, and failures without requiring a hard reset.	Use global defines to inject test errors.

FSW - Path to CDR

CDH

- Develop hardware drivers
- Implement mode switching
- Implement external interfaces (XACT, Li-2, HSTX)
- Define and implement all internal interface packets and commands (EPS, Payload)
- Define data downlink and command uplink packets, opcodes, and payloads

EPS

- Develop hardware drivers
- PPT and SOC calculations
- Commands from and telem to CDH

Documentation

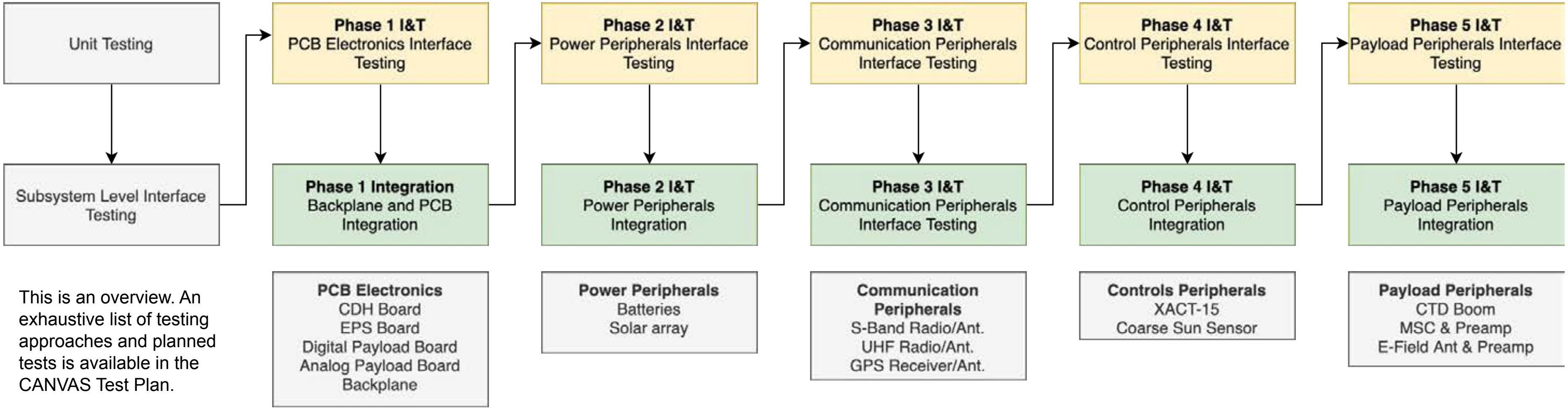
- Command and packet dictionaries
- Introduction to the code
- Pic programming tutorial

System Integration and Testing

Kyle

I&T Overview

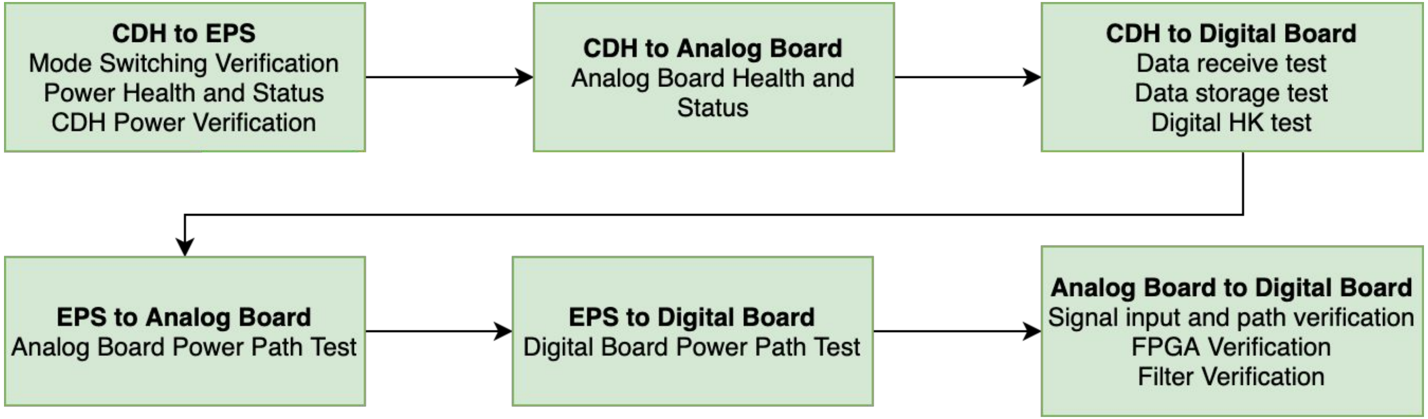
I&T will be completed in phases with each phase adding additional complexity and peripheral equipment to the spacecraft. At this point, all components in subsystems will have been extensively tested at the unit level and interfaced within each subsystem. Environmental testing is done within Phase 2 and Phase 5.



This is an overview. An exhaustive list of testing approaches and planned tests is available in the CANVAS Test Plan.

Phase 1 I&T: PCB Electronics

Interface testing on electronics cards through CANVAS backplane to verify signal and power path through CANVAS PCB stack. Testing will be completed using a regulated, external power supply.



Upon successful completion of interface testing, PCBs will be mounted to the backplane in the CANVAS bus to support further testing and integration.

Phase 2 I&T: Power Peripherals

Testing at this phase is commanded through the CDH board as during normal operations. This phase will test the PCB electronics interface with spacecraft batteries and solar array. Further testing will be done on a regulated, ground power supply metered for load data unless explicitly requiring battery power.

EPS Batteries
Battery charge/discharge test
Battery capacity test
Battery power path test
Battery mode switching
8x Thermal Vacuum

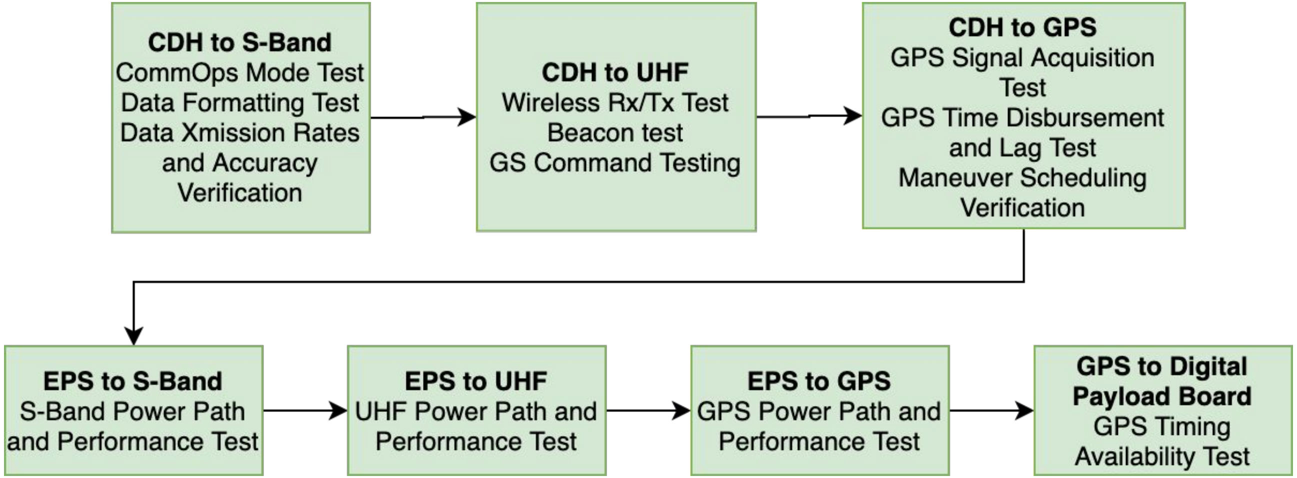
→

EPS Solar Array
Battery charge/discharge test
8x Thermal Vacuum
Deployment testing

Upon completion of the power peripheral interface tests, the bus will be populated with the power peripheral equipment for the remainder of the test phase.

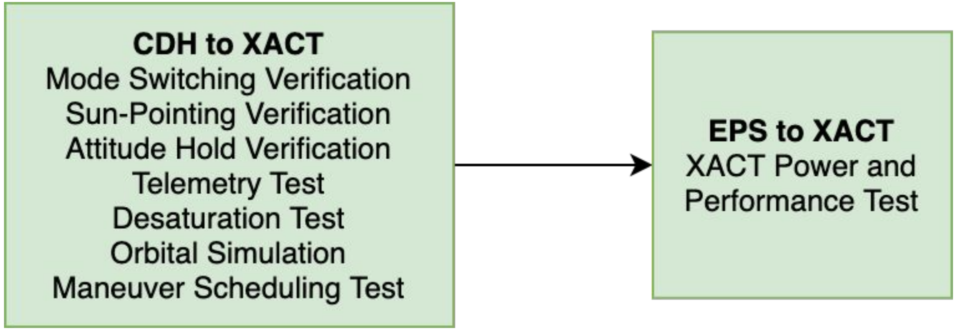
Phase 3 I&T: Communication Peripherals

This phase will test and integrate the S-Band and UHF communication equipment as well as the GPS antenna and receiver. Testing will be commanded via CDH and Flight Software. Power is supplied via external, regulated power supply and metered for power load data.



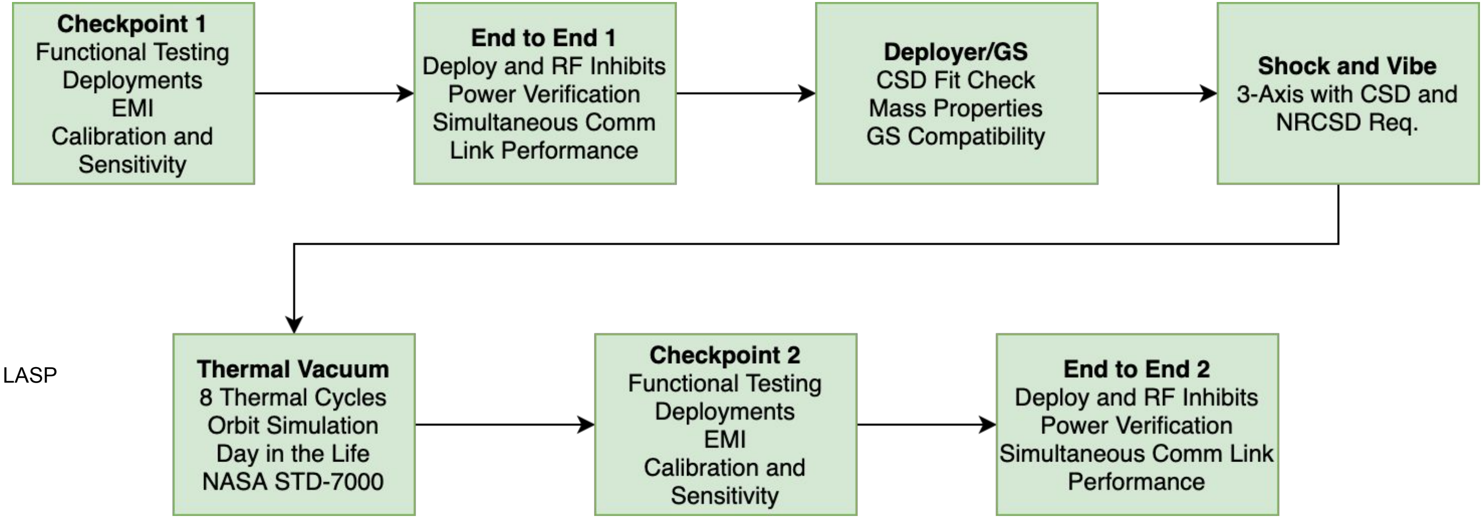
Phase 4 I&T: Control Peripherals

Phase 4 verifies the interface with the XACT and associated sun sensor. Testing with the EDU prior to this stage has verified the signals going into and coming out of the XACT unit. This stage will verify the XACT interface with the rest of the spacecraft.



Phase 5 I&T: Payload Peripherals

Instrumentation I&T is the final phase of integration for the CANVAS spacecraft. This phase includes the most extensive environmental testing as well as end-to-end verification of signal and power pathing and deployments. Successful checkout of this phase moves the spacecraft forward to system-level verification and flight-readiness testing



Ref CIRBE PDR, LASP

Validation and Verification Overview

System Level V&V

The completed satellite will be subject to test and inspection to verify the NRCSD requirements outlined in Chapter 4 of the Nanoracks Interface Control Document. The primary means of system verification will be inspection of spacecraft dimensions and mass properties, analysis and testing given environmental parameters as seen in sections 4.3 and, and inspection and demonstration of applicable safety features in section 4.4. A table of NanoRacks required deliverables is available in section 4.6. The document can be viewed here.

Facilities

Testing	**Facility**
EMI, Shock and Vibe Testing	AERO
Thermal Vacuum Testing	LASP Bemco Chamber (if available)

Support	**Facility**
Ground Station and Operations	LASP
Software and Design Support	LAIR, MAXWELL, RAPs mission

Remaining Integration and Test to CDR

Updates

- Updates to Test Plan and ICDs as subsystem level testing is developed
- Updates to integration approach as subsystem-level testing is completed
- Updates to CONOPs as stated previously
- Updates to Verification and Validation to include on-orbit verification approach

Tracking

- Continue to track budgets through testing and final design phases
- Tracking fulfilment of design requirements in RVM
- Tracking completion of verification deliverables to NanoRacks, see table in NRCSD
- Tracking completion of internal verification

Risk Analysis

Kyle

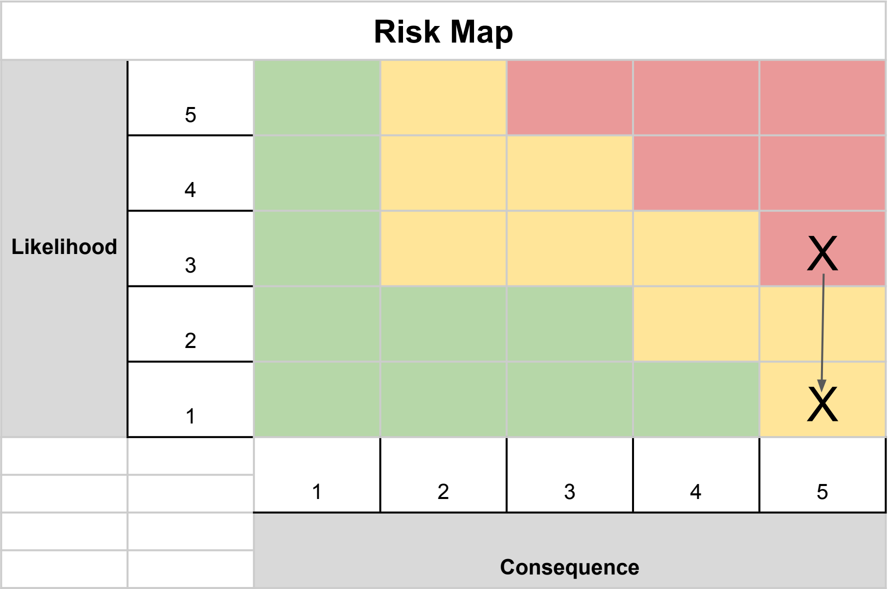
Risks

#	Risk Type	Risk Description	Risk Cause	Likelihood	Consequence
1	Operational	Dependent Deployments	Dependent deployments with no heritage. E-Field antenna and deployment mechanism has not been flown and directly impacts UHF antenna deployment	1	5
2	Operational	CTD Boom Failure	CTD advises against testing boom deployment due to complicated reset process	2	4
3	Design	Data & Link budget overdraw	Volume of science data may exceeds downlink capacity of ground station	2	3
4	Design	Single-Event-Upset Corrupts CDH Memory	The spacecraft is relatively safe from TID, however high-energy particles still pose a risk. With the purpose and volume of science data involved in the CANVAS mission, the consequences are not insignificant.	2	4
5	Design/ Operational	Glint-Free Keep-Out Zone Violation	E-field antenna within the Glint-free keep-out zone reflects light causing the XACT star tracker to lose attitude knowledge. Attitude knowledge then drifts outside the 1 deg accuracy requirement	5	3

This list is not complete. An exhaustive list of risks and mitigation plans associated with the CANVAS mission is available in the Systems and Management Plan (link to PDF)

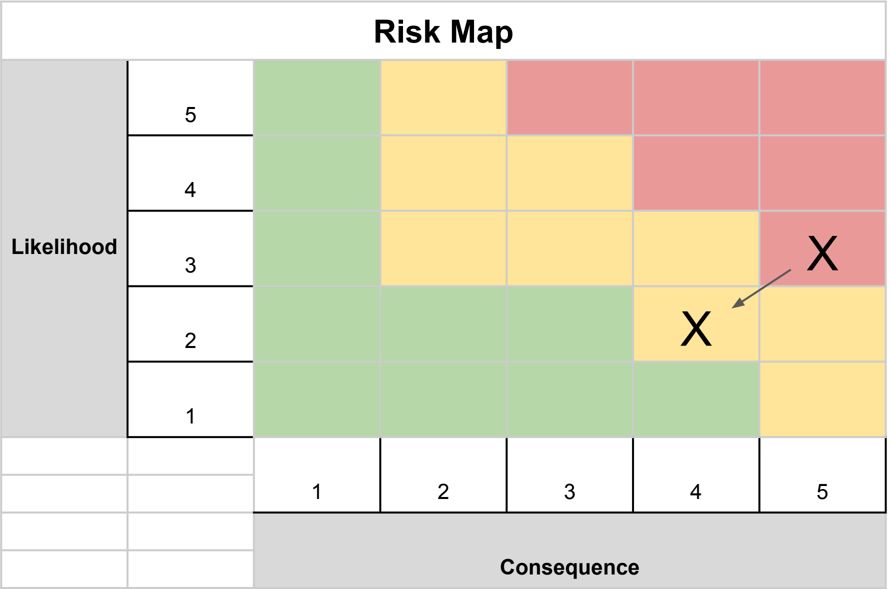
Risk #1 Deployment Dependencies/Failures

Risk Cause	Mitigation
Deployment of UHF depends on successful deployment of E-Field antennas, which depends on successful deployment of Solar Arrays	**Design:** Ensure CDH can continually make deployment attempts until full deployment. Potentially rotate to be sun pointing to burn wires. Design E-Field burn wire mechanism as close to flown solar array design. Potentially use single wire on solar array and E-field **Testing:** Ground based testing of deployments



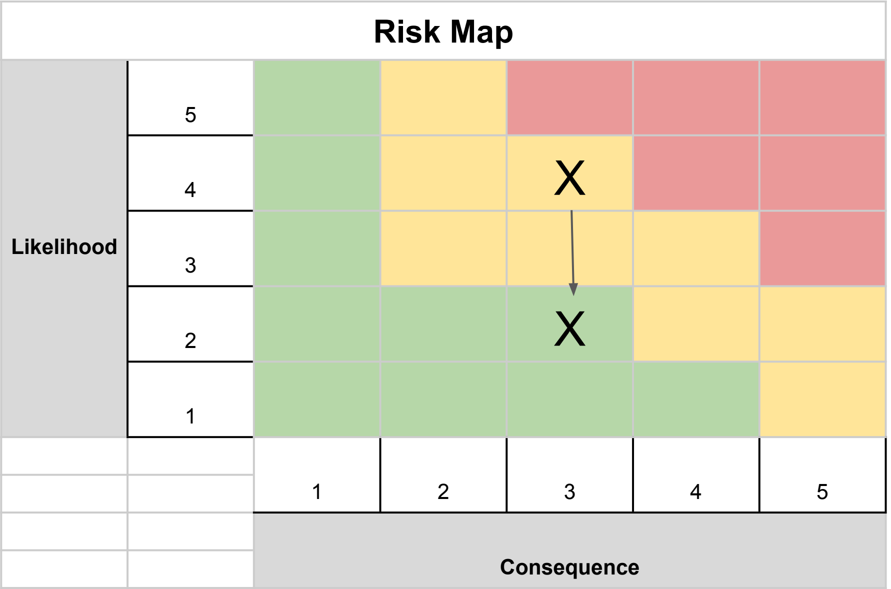
Risk #2 CTD Boom Failure

Risk Cause	Mitigation
CTD Boom has not been flown. CTD advises against customer testing of boom deployment due to complicated reset procedure.	**Design:** Ensure boom is housed properly in structure with clear path to deployment. Design slip ring connections to be free of obstruction **Testing:** Ground based testing of slip ring connections, request video of CTD-run testing, request reset procedure for boom Ensure CDH has capability to retry deployment and store system status and diagnosis



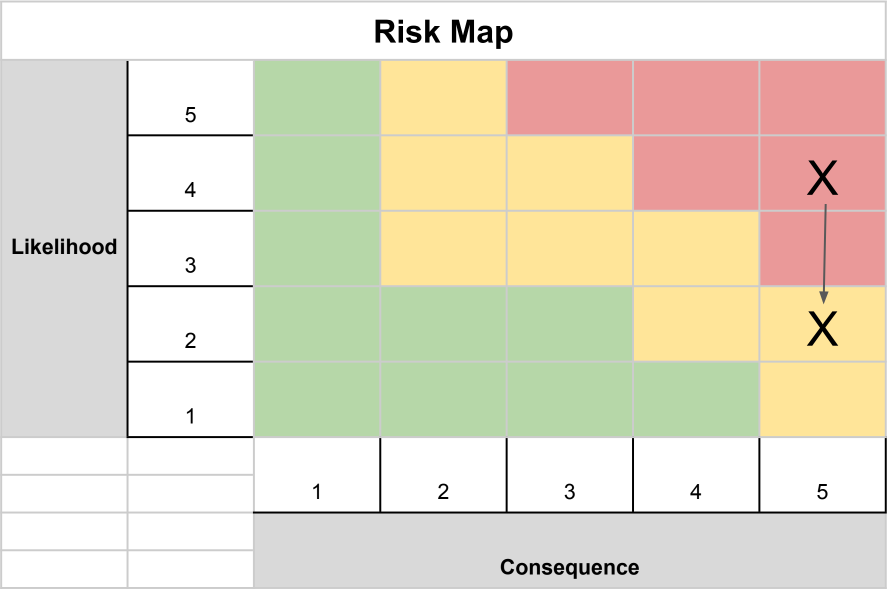
Risk #3 Data and Link Budget Overdraw

Risk Cause	Mitigation
CANVAS mission requires an enormous volume of data to be collected and stored over the course of a 92 minute orbit. A 20 deg elevation mask permits a 5 minute downlink time where the satellite must transmit all onboard data to free up memory for the next orbit. Data transmission bottleneck may overdraw ground station capabilities	**Design:** Ensure spacecraft has data transmission capability with high powered S-Band communication and high accuracy comm pointing mode. Place risk on ground station. May need to reduce size of data through frequency alterations or opportunistic sampling **Testing:** End-to-end RF TX/RX testing for measured data transmission capabilities



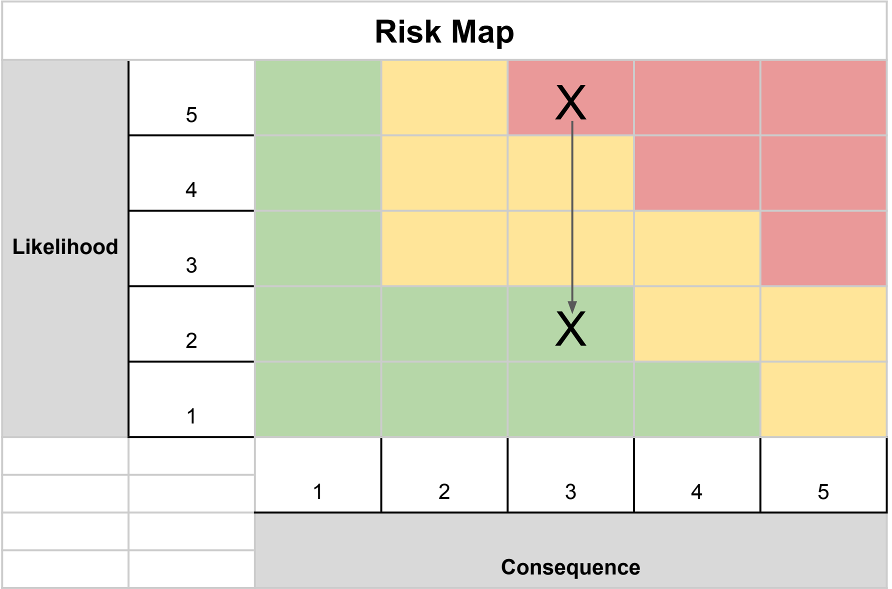
Risk #4 Single Event Upset Memory Corruption

Risk Cause	Mitigation
SEU corruption of on-board memory poses significant consequences to the CANVAS mission due to the large volume of science data being handled on-board	**Design:** Redundant, identical memory storage units



Risk #5 Glint-Free Keep-Out Zone Violation

Risk Cause	Mitigation
E-field antenna within the Glint-free keep-out zone reflects light causing the XACT star tracker to lose attitude knowledge. Attitude knowledge then drifts outside the 1 deg accuracy requirement	**Design:** Coat E-field antennas with DAG213. **Testing:** Ensure the scientific integrity of antennas are not compromised through testing.



Schedule and Budget

Kyle

University of Colorado Boulder

Budget

Total HW Budget:

$300,000

Budgeted:

$297,100

Spent:
$251,309.46

Remaining:

$48,690.54

Subsystem	Item	Point of Contact	Budgeted	Contingency	Expected Cost	Spent	Remaining
ADCS	Blue Canyon XACT and EDU	Kyle	$ 150,000.00	0%	$ 150,000.00	$ 150,000.00	$ -
INST	Novatel GPS Receiver	Arvind	$ 3,200.00	25%	$ 4,000.00	$ -	$ 4,000.00
INST	E-field Pre-Amp Rev1	Riley	$ 106.68	0%	$ 106.68	$ 106.68	$ -
INST	E-field Pre-Amp Rev2	Riley	$ 73.83	0%	$ 73.83	$ 73.83	$ -
INST	E-field Pre-Amp Rev3	Riley	$ 150.00	10%	$ 165.00	$ -	$ 165.00
INST	E-field Pre-Amp Flight	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	B-field Pre-Amp Rev1	Riley	$ 300.00	25%	$ 375.00	$ 180.41	$ 194.59
INST	B-field Pre-Amp Rev2	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	B-field Pre-Amp Rev3	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	B-field Pre-Amp Flight	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	Analog Bread Board Testing	Riley	$ 500.00	25%	$ 625.00	$ 207.24	$ 417.76
INST	Analog Rev 1	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	Analog Rev 2	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	Analog Rev 3	Riley	$ 200.00	25%	$ 250.00	$ -	$ 250.00
INST	Analog Flight	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	Digital Rev 1	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	Digital Rev 2	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	Digital Rev 3	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	Digital Flight	Riley	$ 300.00	25%	$ 375.00	$ -	$ 375.00
INST	FPGA	Arvind	$ 3,500.00	25%	$ 4,375.00	$ -	$ 4,375.00
INST	Misc. Electronics Parts	Riley	$ 1,500.00	25%	$ 1,875.00	$ 62.57	$ 1,812.43
MECH/INST	E-Field Antennas	Gautham/Mayank	$ 500.00	25%	$ 625.00	$ 50.73	$ 574.27
MECH/INST	Search Coils	Arvind/Riley	$ -	0%	$ -	$ -	$ -
MECH/INST	CTD boom deployer	Kyle/Riley/Tucker	$ 85,000.00	0%	$ 85,000.00	$ 85,000.00	$ -

Budget

Total HW Budget:

$300,000

Budgeted:

$297,100

Spent:
$251,309.46

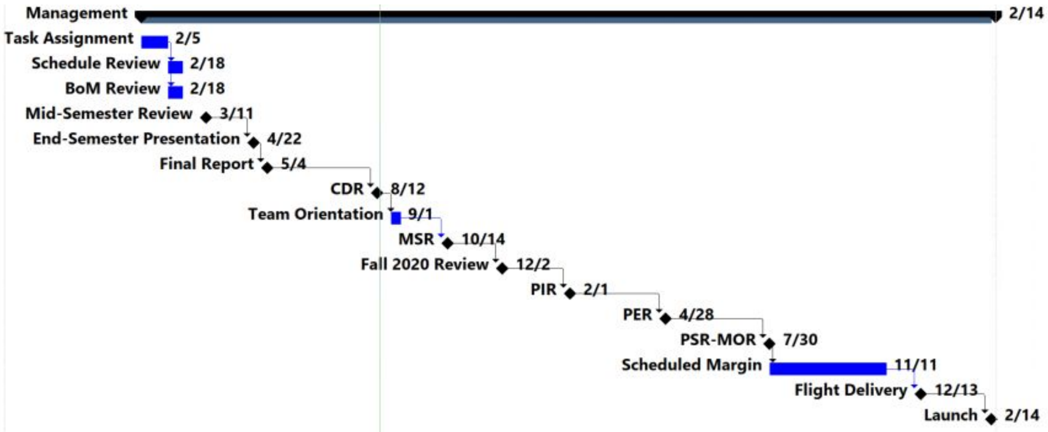
Remaining:

$48,690.54

Subsystem	Item	Point of Contact	Budgeted	Contingency	Expected Cost	Spent	Remaining
MECH	Structure Panels	Dhruv	$ 1,500.00	50%	$ 2,250.00	$ -	$ 2,250.00
MECH		Dhruv	$ -	0%	$ -	$ -	$ -
MECH	PEEK for B-Field Payload	Alexei	$ 2,500.00	10%	$ 2,750.00	$ -	$ 2,750.00
MECH	Misc. Mechanical componants	Dhruv	$ 2,000.00	10%	$ 2,200.00	$ -	$ 2,200.00
MECH	3D Printing (Fit-check prototyping)	Dhruv	$ 150.00	10%	$ 165.00	$ -	$ 165.00
COMM	UHF Radio	Cara	$ 5,000.00	5%	$ 5,250.00	$ -	$ 5,250.00
COMM	UHF Daughter Board	Cara	$ 250.00	10%	$ 275.00	$ -	$ 275.00
COMM	S-band Radio	Cara	$ 11,250.00	0%	$ 11,250.00	$ 11,250.00	$ -
COMM	S-band Daughter Board	Jett	$ 200.00	10%	$ 220.00	$ -	$ 220.00
COMM	UHF Antenna	Cara/Dhruv	$ 700.00	10%	$ 770.00	$ -	$ 770.00
COMM	S-band Antenna	Cara	$ 4,253.00	0%	$ 4,253.00	$ 4,253.00	$ -
COMM	Shipping	Cara	$ 250.00	0%	$ 250.00	$ 125.00	$ 125.00
EPS	Solar cells and panels	Connor	$ 11,000.00	15%	$ 12,650.00	$ -	$ 12,650.00
EPS	Battery	Connor	$ 72.00	50%	$ 108.00	$ -	$ 108.00
EPS	EPS Rev 1	Connor	$ 300.00	10%	$ 330.00	$ -	$ 330.00
EPS	EPS Rev 2	Connor	$ 300.00	10%	$ 330.00	$ -	$ 330.00
EPS	EPS Rev 3	Connor	$ 300.00	10%	$ 330.00	$ -	$ 330.00
EPS	EPS Flight Board	Connor	$ 500.00	10%	$ 550.00	$ -	$ 550.00
EPS	Bus wires & connectors	Connor	$ 300.00	10%	$ 330.00	$ -	$ 330.00
C&DH	Back Plane Rev 1	Jett	$ 150.00	10%	$ 165.00	$ -	$ 165.00
C&DH	Back Plane Rev 2	Jett	$ 150.00	10%	$ 165.00	$ -	$ 165.00
C&DH	CDH Rev 1	Chadd	$ 300.00	10%	$ 330.00	$ -	$ 330.00
C&DH	CDH Rev 2	Chadd	$ 300.00	10%	$ 330.00	$ -	$ 330.00
C&DH	CDH Rev 3	Chadd	$ 300.00	10%	$ 330.00	$ -	$ 330.00
C&DH	CHD Flight Board	Chadd	$ 500.00	10%	$ 550.00	$ -	$ 550.00
		TOTAL	$ 290,355.51	$ 6,746.00	$ 297,101.51	$ 251,309.46	$ 48,690.54
		Margin	$ 9,644.49		$ 2,898.49		
			19.81	%	5.96	%	

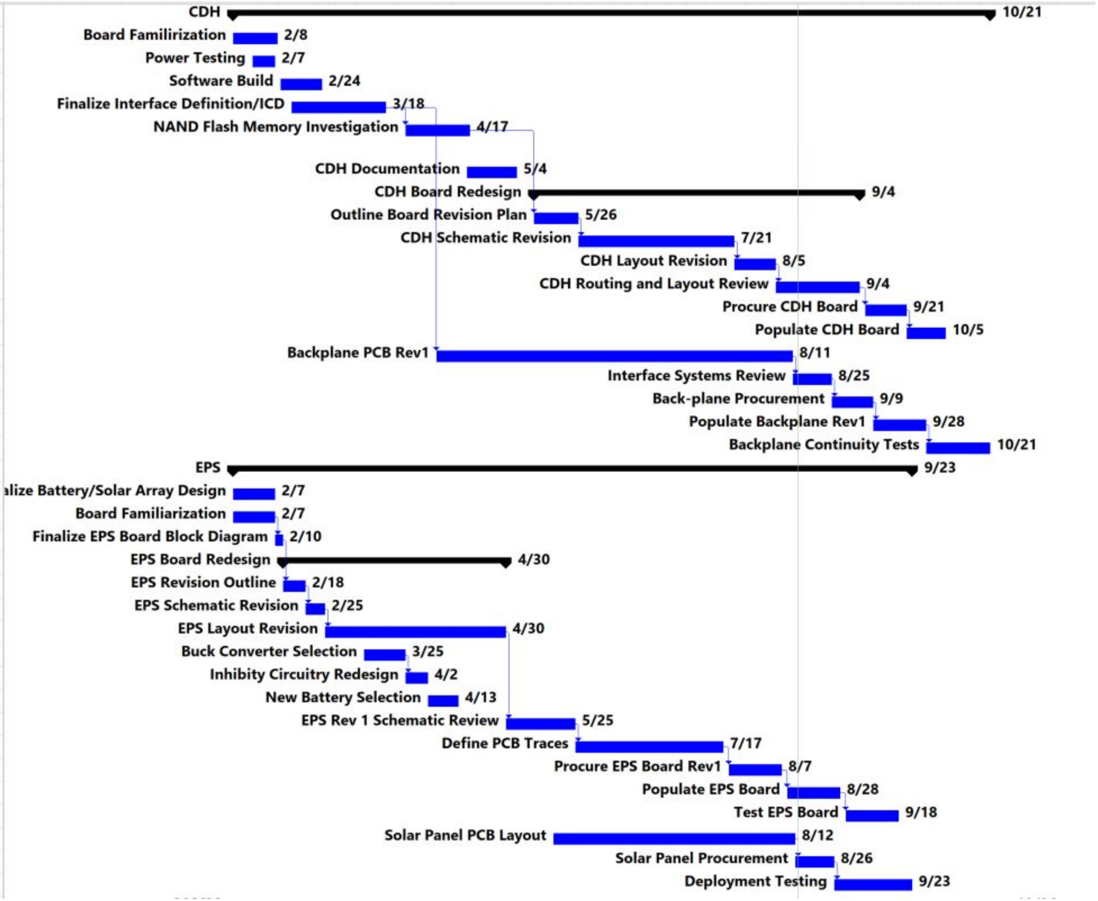
Schedule - Overview

Management	**550 days**	**1/13/20**	**2/17/22**	
Task Assignment	18 days	1/13/20	2/5/20	
Schedule Review	10 days	2/6/20	2/18/20	47
BoM Review	10 days	2/6/20	2/18/20	47
Mid-Semester Review	0 days	3/11/20	3/11/20	
End-Semester Presentation	0 days	4/22/20	4/22/20	50
Final Report	0 days	5/4/20	5/4/20	51
CDR	0 days	8/12/20	8/12/20	52
Team Orientation	7 days	8/24/20	9/1/20	53
MSR	0 days	10/14/20	10/14/20	54
Fall 2020 Review	0 days	12/2/20	12/2/20	55
PIR	0 days	2/1/21	2/1/21	56
PER	0 days	4/28/21	4/28/21	57
PSR-MOR	0 days	7/30/21	7/30/21	58
Scheduled Margin	75 days	7/30/21	11/11/21	59
Flight Delivery	0 days	12/13/21	12/13/21	60
Launch	0 days	2/14/22	2/14/22	61



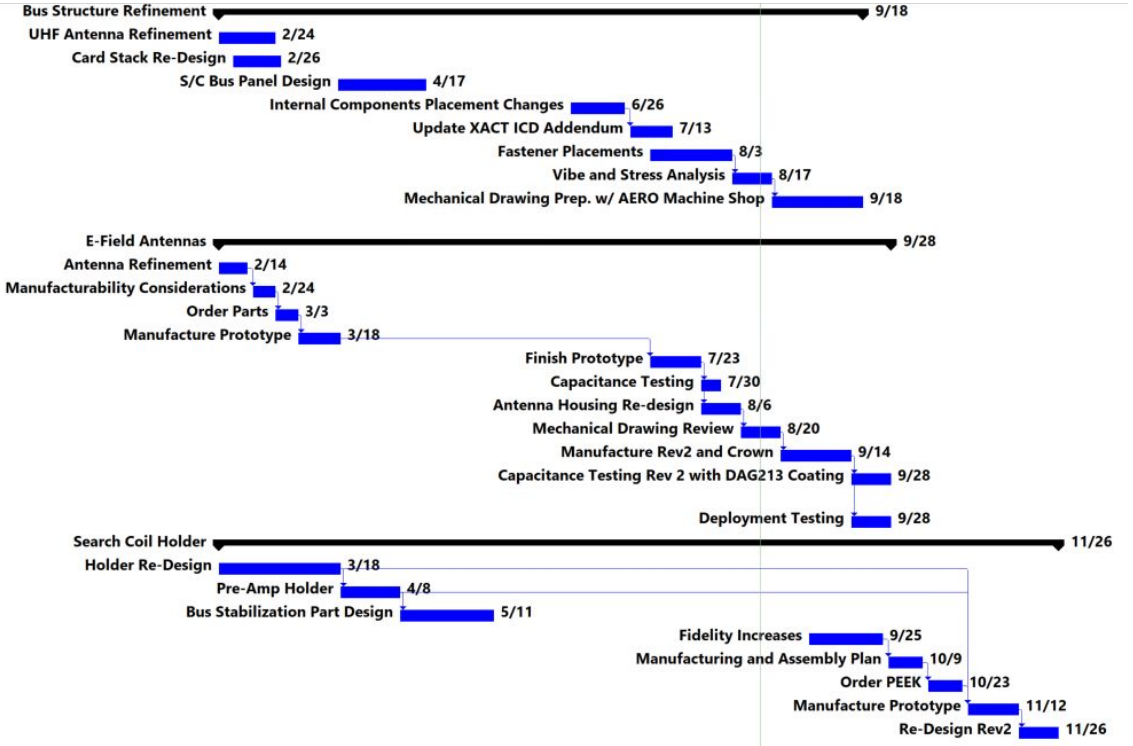
Schedule - CHD and EPS

CDH	195 days?	1/24/20	10/21/20	
Board Familirization	12 days	1/24/20	2/8/20	
Power Testing	6 days	1/31/20	2/7/20	
Software Build	11 days	2/10/20	2/24/20	
Finalize Interface Definition/ICD	24 days	2/14/20	3/18/20	
NAND Flash Memory Investigation	17 days	3/26/20	4/17/20	67
CDH Documentation	12 days?	4/17/20	5/4/20	
CDH Board Redesign	**85 days**	**5/11/20**	**9/4/20**	
Outline Board Revision Plan	12 days	5/11/20	5/26/20	68
CDH Schematic Revision	40 days	5/27/20	7/21/20	71
CDH Layout Revision	11 days	7/22/20	8/5/20	72
CDH Routing and Layout Review	22 days	8/6/20	9/4/20	73
Procure CDH Board	11 days	9/7/20	9/21/20	74
Populate CDH Board	10 days	9/22/20	10/5/20	75
Backplane PCB Rev1	92 days	4/6/20	8/11/20	67
Interface Systems Review	10 days	8/12/20	8/25/20	77
Back-plane Procurement	11 days	8/26/20	9/9/20	78
Populate Backplane Rev1	13 days?	9/10/20	9/28/20	79
Backplane Continuity Tests	17 days	9/29/20	10/21/20	80
EPS	175 days?	1/24/20	9/23/20	
Finalize Battery/Solar Array Design	11 days	1/24/20	2/7/20	
Board Familiarization	11 days	1/24/20	2/7/20	
Finalize EPS Board Block Diagram	2 days	2/8/20	2/10/20	84
EPS Board Redesign	**58 days?**	**2/11/20**	**4/30/20**	
EPS Revision Outline	6 days	2/11/20	2/18/20	85
EPS Schematic Revision	5 days	2/19/20	2/25/20	87
EPS Layout Revision	47 days	2/26/20	4/30/20	88
Buck Converter Selection	11 days?	3/11/20	3/25/20	
Inhibity Circuitry Redesign	6 days	3/26/20	4/2/20	90
New Battery Selection	7 days?	4/3/20	4/13/20	
EPS Rev 1 Schematic Review	17 days	5/1/20	5/25/20	89
Define PCB Traces	39 days	5/26/20	7/17/20	93
Procure EPS Board Rev1	15 days	7/20/20	8/7/20	94
Populate EPS Board	15 days	8/10/20	8/28/20	95
Test EPS Board	15 days	8/31/20	9/18/20	96
Solar Panel PCB Layout	63 days	5/18/20	8/12/20	
Solar Panel Procurement	10 days	8/13/20	8/26/20	98
Deployment Testing	20 days	8/27/20	9/23/20	99



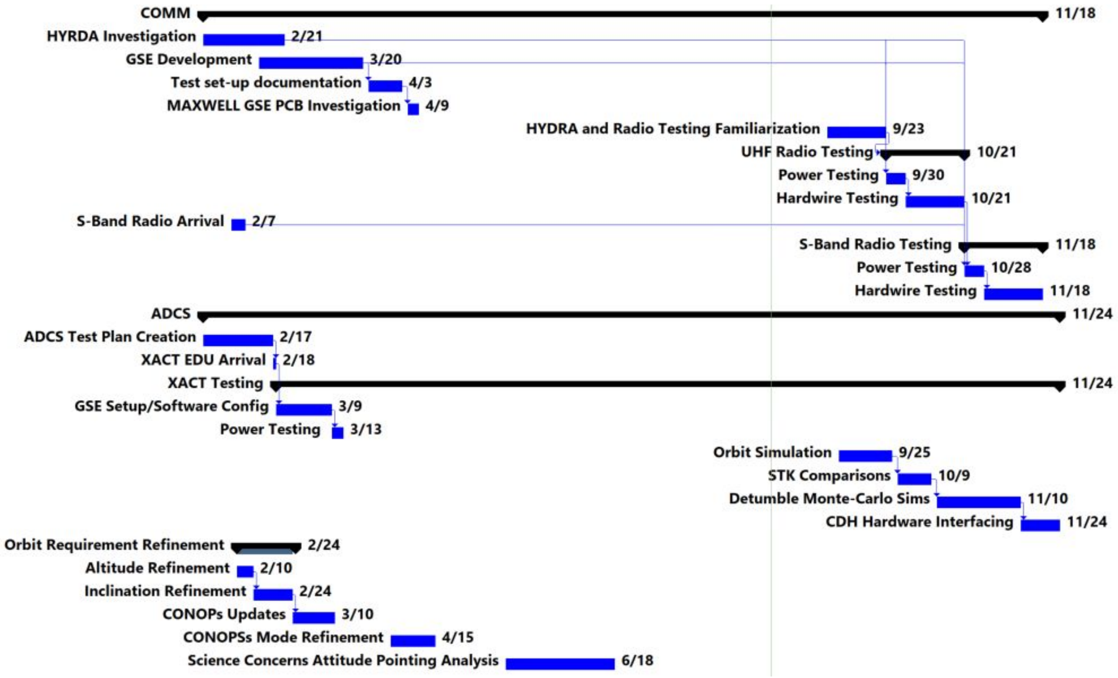
Schedule - Structures

Bus Structure Refinement	**164 days?**	**2/5/20**	**9/18/20**	
UHF Antenna Refinement	15 days	2/5/20	2/24/20	
Card Stack Re-Design	13 days	2/10/20	2/26/20	
S/C Bus Panel Design	23 days?	3/18/20	4/17/20	
Internal Components Placement Changes	15 days	6/8/20	6/26/20	
Update XACT ICD Addendum	11 days	6/29/20	7/13/20	146
Fastener Placements	21 days	7/6/20	8/3/20	
Vibe and Stress Analysis	10 days	8/4/20	8/17/20	148
Mechanical Drawing Prep. w/ AERO Machine Shop	24 days	8/18/20	9/18/20	149
E-Field Antennas	**170 days**	**2/5/20**	**9/28/20**	
Antenna Refinement	9 days	2/5/20	2/14/20	
Manufacturability Considerations	6 days	2/17/20	2/24/20	152
Order Parts	6 days	2/25/20	3/3/20	153
Manufacture Prototype	11 days	3/4/20	3/18/20	154
Finish Prototype	14 days	7/6/20	7/23/20	155
Capacitance Testing	5 days	7/24/20	7/30/20	156
Antenna Housing Re-design	10 days	7/24/20	8/6/20	156
Mechanical Drawing Review	10 days	8/7/20	8/20/20	158
Manufacture Rev2 and Crown	17 days	8/21/20	9/14/20	159
Capacitance Testing Rev 2 with DAG213 Coating	10 days	9/15/20	9/28/20	160
Deployment Testing	10 days	9/15/20	9/28/20	160
Search Coil Holder	**213 days**	**2/5/20**	**11/26/20**	
Holder Re-Design	32 days	2/5/20	3/18/20	
Pre-Amp Holder	15 days	3/19/20	4/8/20	164
Bus Stabilization Part Design	23 days	4/9/20	5/11/20	165
Fidelity Increases	20 days	8/31/20	9/25/20	
Manufacturing and Assembly Plan	10 days	9/28/20	10/9/20	167
Order PEEK	10 days	10/12/20	10/23/20	168
Manufacture Prototype	14 days	10/26/20	11/12/20	169,1
Re-Design Rev2	10 days	11/13/20	11/26/20	170



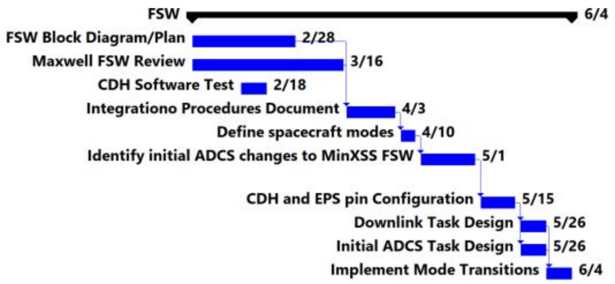
Schedule - ADCS and COMMs

COMM	**215 days**	**1/24/20**	**11/18/20**	
HYRDA Investigation	22 days	1/24/20	2/21/20	
GSE Development	27 days	2/13/20	3/20/20	
Test set-up documentation	10 days	3/23/20	4/3/20	103
MAXWELL GSE PCB Investigation	4 days	4/6/20	4/9/20	104
HYDRA and Radio Testing Familiarization	15 days	9/3/20	9/23/20	
UHF Radio Testing	**20 days**	**9/24/20**	**10/21/20**	**106**
Power Testing	5 days	9/24/20	9/30/20	103,1
Hardwire Testing	15 days	10/1/20	10/21/20	108
S-Band Radio Arrival	5 days	2/3/20	2/7/20	
S-Band Radio Testing	**20 days**	**10/22/20**	**11/18/20**	
Power Testing	5 days	10/22/20	10/28/20	110,1
Hardwire Testing	15 days	10/29/20	11/18/20	112
ADCS	**219 days?**	**1/24/20**	**11/24/20**	
ADCS Test Plan Creation	18 days	1/24/20	2/17/20	
XACT EDU Arrival	1 day	2/18/20	2/18/20	115
XACT Testing	**200 days**	**2/19/20**	**11/24/20**	
GSE Setup/Software Config	14 days	2/19/20	3/9/20	116
Power Testing	4 days	3/10/20	3/13/20	118
Orbit Simulation	15 days	9/7/20	9/25/20	
STK Comparisons	10 days	9/28/20	10/9/20	120
Detumble Monte-Carlo Sims	22 days	10/12/20	11/10/20	121
CDH Hardware Interfacing	10 days	11/11/20	11/24/20	122
Orbit Requirement Refinement	**16 days?**	**2/5/20**	**2/25/20**	
Altitude Refinement	5 days?	2/5/20	2/10/20	
Inclination Refinement	10 days	2/11/20	2/24/20	125
CONOPs Updates	11 days	2/25/20	3/10/20	126
CONOPSs Mode Refinement	12 days?	3/31/20	4/15/20	
Science Concerns Attitude Pointing Analysis	29 days	5/11/20	6/18/20	



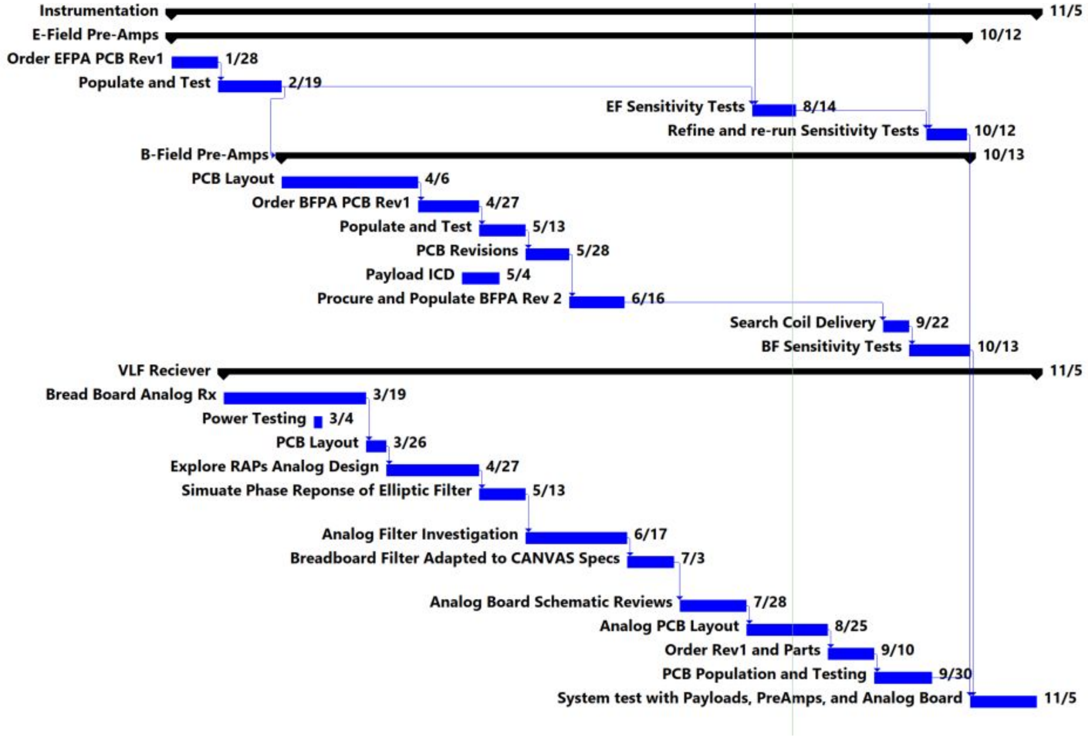
Schedule - FSW

FSW	**96 days**	**1/24/20**	**6/4/20**	
FSW Block Diagram/Plan	27 days	1/24/20	2/28/20	
Maxwell FSW Review	38 days	1/24/20	3/16/20	
CDH Software Test	7 days	2/10/20	2/18/20	65
Integrationo Procedures Document	13 days	3/18/20	4/3/20	131,1
Define spacecraft modes	5 days	4/6/20	4/10/20	134
Identify initial ADCS changes to MinXSS FSW	15 days	4/13/20	5/1/20	135
CDH and EPS pin Configuration	10 days	5/4/20	5/15/20	136
Downlink Task Design	7 days	5/18/20	5/26/20	137
Initial ADCS Task Design	7 days	5/18/20	5/26/20	137
Implement Mode Transitions	7 days	5/27/20	6/4/20	139,1



Schedule - Instrumentation

Instrumentation	**215 days**	**1/13/20**	**11/5/20**	
E-Field Pre-Amps	**197 days**	**1/13/20**	**10/12/20**	
Order EFPA PCB Rev1	12 days	1/13/20	1/28/20	
Populate and Test	17 days	1/29/20	2/19/20	179
EF Sensitivity Tests	11 days	7/31/20	8/14/20	180,1
Refine and re-run Sensitivity Tests	10 days	9/29/20	10/12/20	161,1
B-Field Pre-Amps	**169 days**	**2/20/20**	**10/13/20**	**180**
PCB Layout	33 days	2/20/20	4/6/20	
Order BFPA PCB Rev1	15 days	4/7/20	4/27/20	184
Populate and Test	12 days	4/28/20	5/13/20	185
PCB Revisions	11 days	5/14/20	5/28/20	186
Payload ICD	9 days	4/22/20	5/4/20	
Procure and Populate BFPA Rev 2	13 days	5/29/20	6/16/20	187
Search Coil Delivery	7 days	9/14/20	9/22/20	189
BF Sensitivity Tests	15 days	9/23/20	10/13/20	190
VLF Reciever	**201 days**	**1/31/20**	**11/5/20**	
Bread Board Analog Rx	36 days	1/31/20	3/19/20	
Power Testing	3 days	3/2/20	3/4/20	
PCB Layout	5 days	3/20/20	3/26/20	193
Explore RAPs Analog Design	22 days	3/27/20	4/27/20	195
Simuate Phase Reponse of Elliptic Filter	12 days	4/28/20	5/13/20	196
Analog Filter Investigation	25 days	5/14/20	6/17/20	197
Breadboard Filter Adapted to CANVAS Specs	12 days	6/18/20	7/3/20	198
Analog Board Schematic Reviews	17 days	7/6/20	7/28/20	199
Analog PCB Layout	20 days	7/29/20	8/25/20	200
Order Rev1 and Parts	12 days	8/26/20	9/10/20	201
PCB Population and Testing	14 days	9/11/20	9/30/20	202
System test with Payloads, PreAmps, and Analog Board	17 days	10/14/20	11/5/20	203,1



CANVAS
Summer 2020 Review

References

References

Lefeuvre, F., R. Marshall, J. L. Pincon, U. S. Inan, D. Lagoutte, M. Parrot, and J.-J. Berthelier (2009), On remote sensing of transient luminous events' parent lightning discharges by ELF/VLF wave measurements on board a satellite, *J. Geophys. Res.*, *in press*, doi:10.1029/2009JA014154.

Hospodarsky, G. B. (2016), Spaced-based search coil magnetometers, *J. Geophys. Res. Space Physics*, 121, 12,068– 12,079, doi:10.1002/2016JA022565.

Santolík, O., M. Parrot, and F. Lefeuvre (2003), Singular value decomposition methods for wave propagation analysis, *Radio Science*, *38*(1).

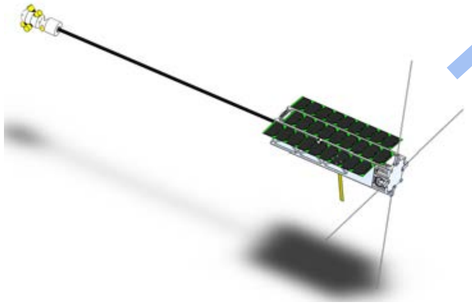
Backup Slides

CANVAS data product

3 **real** magnetic field components, continuously collected

+

2 **real** electric field components, continuously collected



onboard FFT:

- 1 spectra/second
- 67 frequency bins

5 **complex** amplitudes

$$Q = \begin{bmatrix} c^2 B_1 B_1^* & c^2 B_1 B_2^* & c^2 B_1 B_3^* & cB_1 E_1^* & cB_1 E_2^* \\ c^2 B_2 B_1^* & c^2 B_2 B_2^* & c^2 B_2 B_3^* & cB_2 E_1^* & cB_2 E_2^* \\ c^2 B_3 B_1^* & c^2 B_3 B_2^* & c^2 B_3 B_3^* & cB_3 E_1^* & cB_3 E_2^* \\ cE_1 B_1^* & cE_1 B_2^* & cE_1 B_3^* & E_1 E_1^* & E_1 E_2^* \\ cE_2 B_1^* & cE_2 B_2^* & cE_2 B_3^* & E_2 E_1^* & E_2 E_2^* \end{bmatrix}$$

Transmit 5 diagonal values and 10 off-diagonal complex values

Faraday's Law:
k x **E** = ω**B**

Re(E) • Re(B) = 0
Im(E) • Im(B) = 0

6x6 Spectral Matrix Q per frequency bin w/ time resolution of 1 second

University of Colorado **Boulder**

Reference: Santolik, et. al.

Singular Value Decomposition

Faraday's Law:

- **k** x **E** = ω**B**
- **n** x **E** = c**B**
    - **n** = **k**c/ω

A and b composed from:

$$\boxed{\sum_{j,k=1}^{3} \epsilon_{ijk}\, E_k\, \zeta_\ell^*\, n_j} = \boxed{c\, B_i\, \zeta_\ell^*,}\quad i = 1\ldots3,\ \ell = 1\ldots6,$$

- where: $\zeta = (cB_1, cB_2, cB_3, E_1, E_2, E_3)$
- Real and imaginary forms of A stacked into 36x3 matrix
- Real and imaginary forms of b stacked into 36x1

$$\begin{bmatrix} 0 & Q_{6,1} & -Q_{5,1} \\ -Q_{6,1} & 0 & Q_{4,1} \\ Q_{5,1} & -Q_{4,1} & 0 \\ 0 & Q_{6,2} & -Q_{5,2} \\ -Q_{6,2} & 0 & Q_{4,2} \\ Q_{5,2} & -Q_{4,2} & 0 \\ 0 & Q_{6,3} & -Q_{5,3} \\ -Q_{6,3} & 0 & Q_{4,3} \\ Q_{5,3} & -Q_{4,3} & 0 \\ & \cdot & \\ & \cdot & \\ & \cdot & \\ & \cdot & \\ 0 & Q_{6,6} & -Q_{5,6} \\ -Q_{6,6} & 0 & Q_{4,6} \\ Q_{5,6} & -Q_{4,6} & 0 \end{bmatrix}$$

$$\begin{bmatrix} Q_{1,1} \\ Q_{2,1} \\ Q_{3,1} \\ Q_{1,2} \\ Q_{2,2} \\ Q_{3,2} \\ \cdot \\ \cdot \\ Q_{2,6} \\ Q_{3,6} \end{bmatrix}$$

Matrix eqn: **A • n = b**

SVD:
A = U • W • V^T

n = V • W^(-1) • U^T • b

- Solve for n to get k vector direction

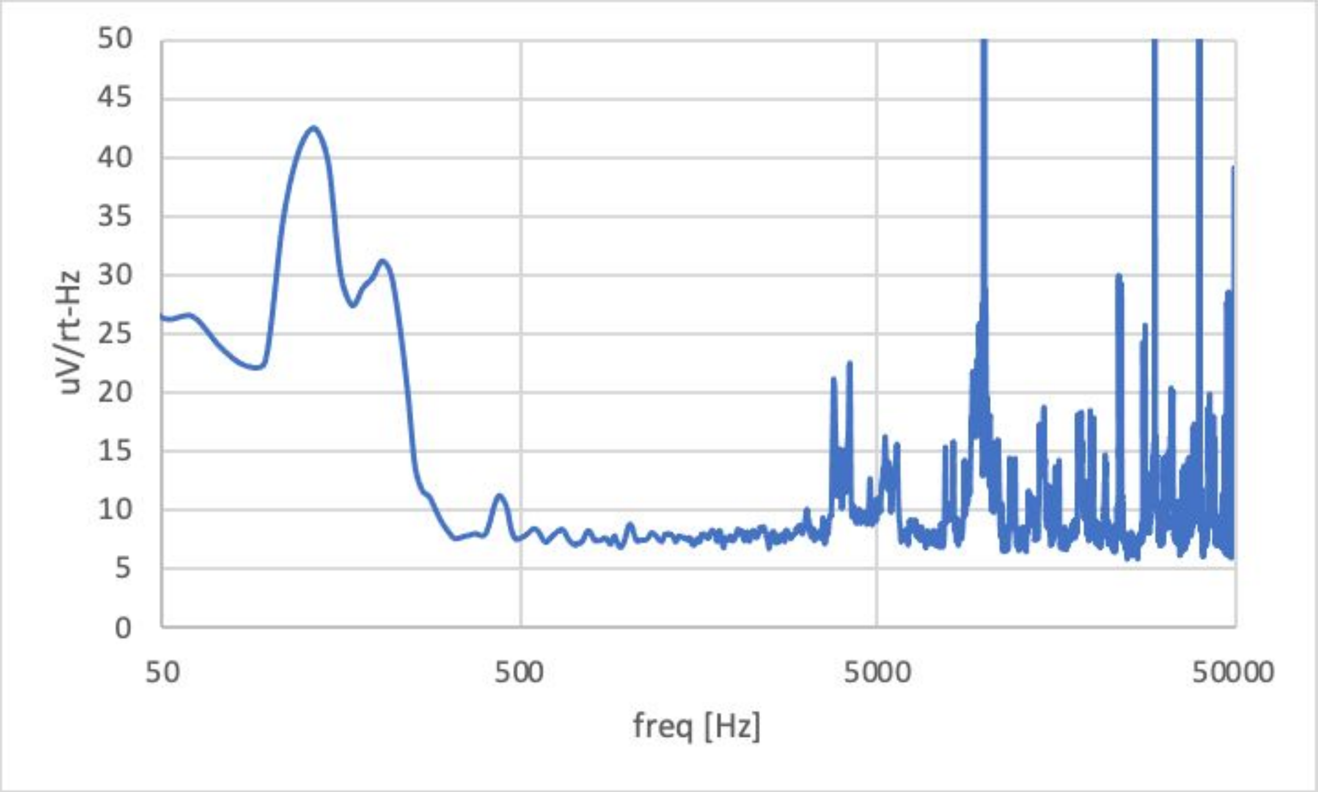
- Can also get planarity, polarization, antenna gain..

E-Field Preamp- Sensitivity Testing w/ Antenna rev 1

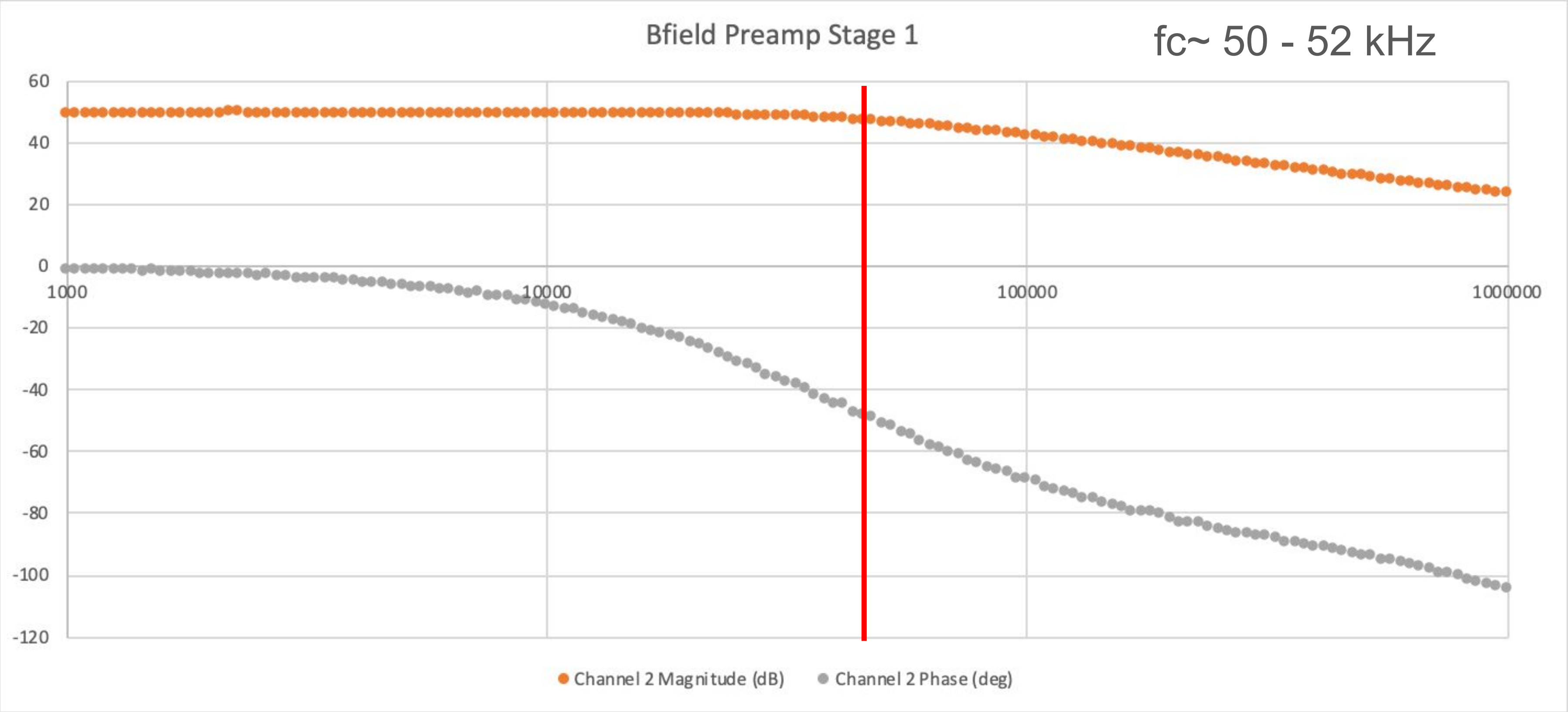
SCI-1.2:
Measure E fields with sensitivity less than 10^-6 V/m/rt-Hz in the band of interest

Next steps to improve:
Obtain faraday cage and low noise spectrum analyzer to accurately determine noise floor

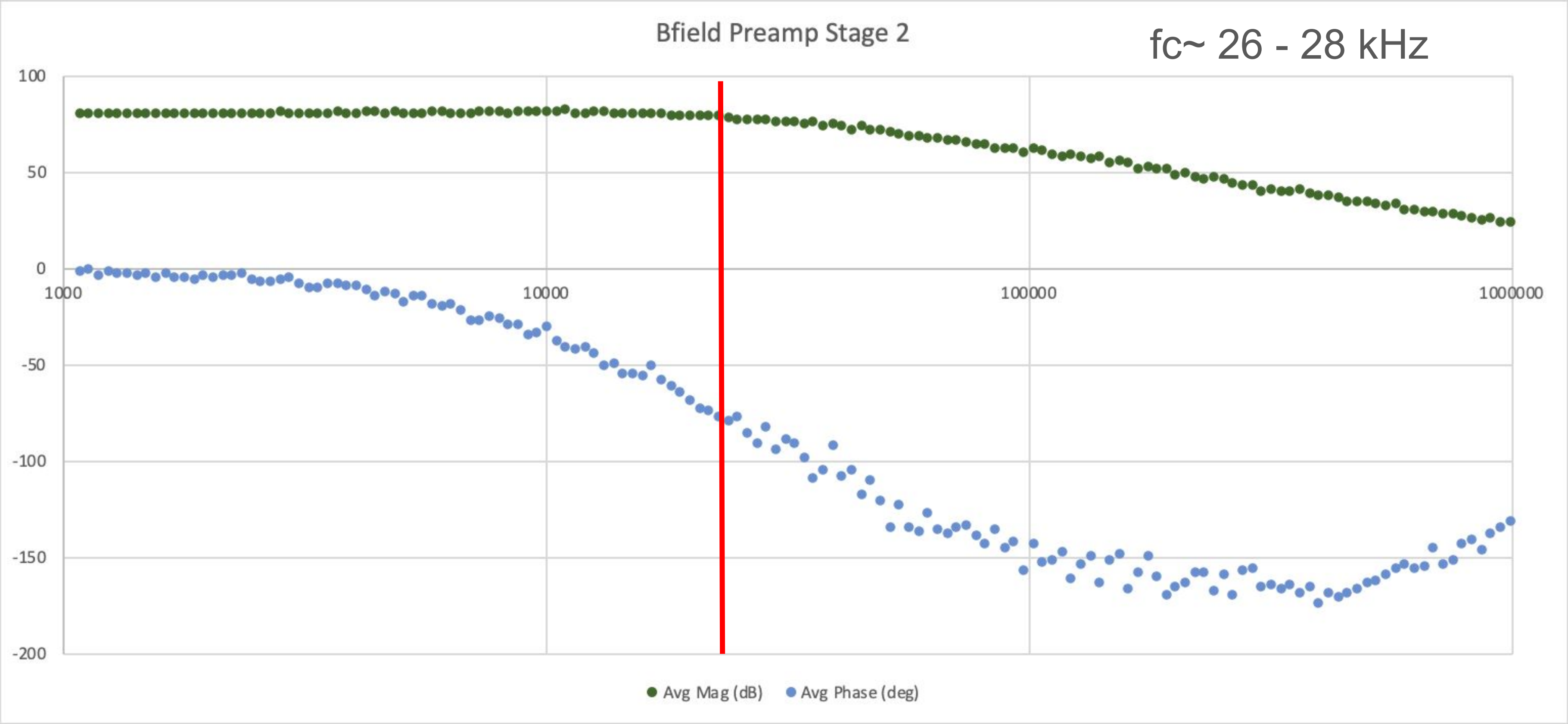
Use higher fidelity instruments (not Analog Discovery) to record any detected signals



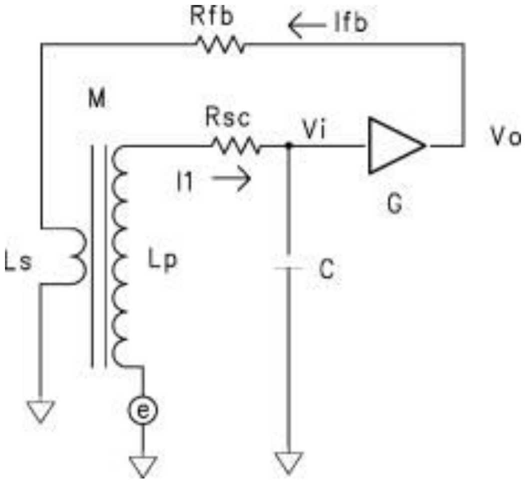
B-Field Preamp - Status



B-Field Preamp - Status



B-Field Preamp - Status

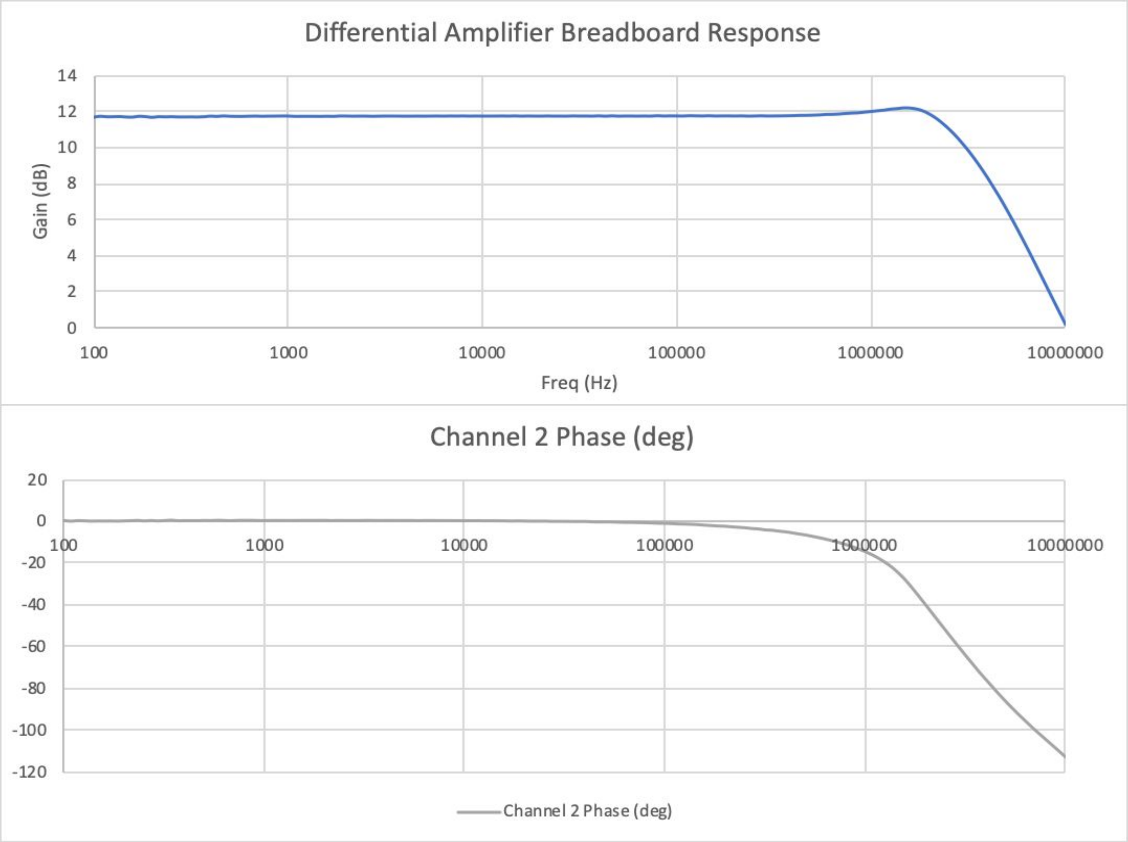


H. C. Séran and P. Fergeau, 2005
DEMETER search coil paper

- Suggestions from Guillaume Jannet at CNRS guide our next steps to adjusting the filter response by tuning passive values in the second stage
  - Search coils arrive ~ September

Analog Board - Status- Differential Amplifier

- Differential Amplifier
  - Uses RAPS Design
  - Op Amp: OPA1656
- Breadboard results

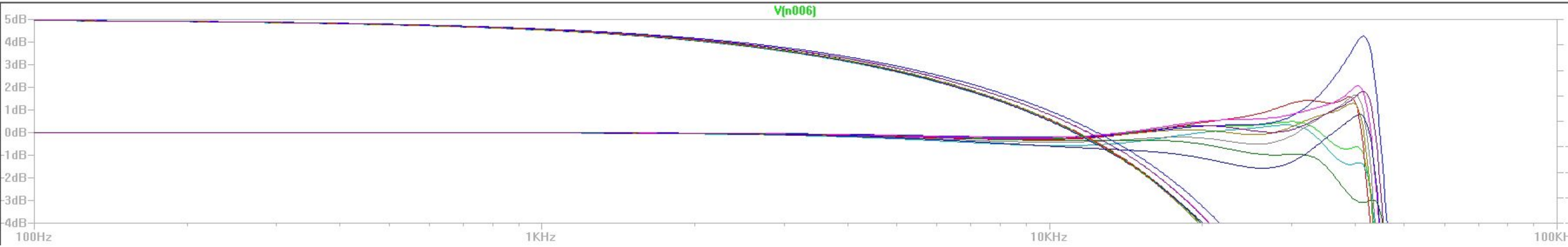


Analog board breadboard

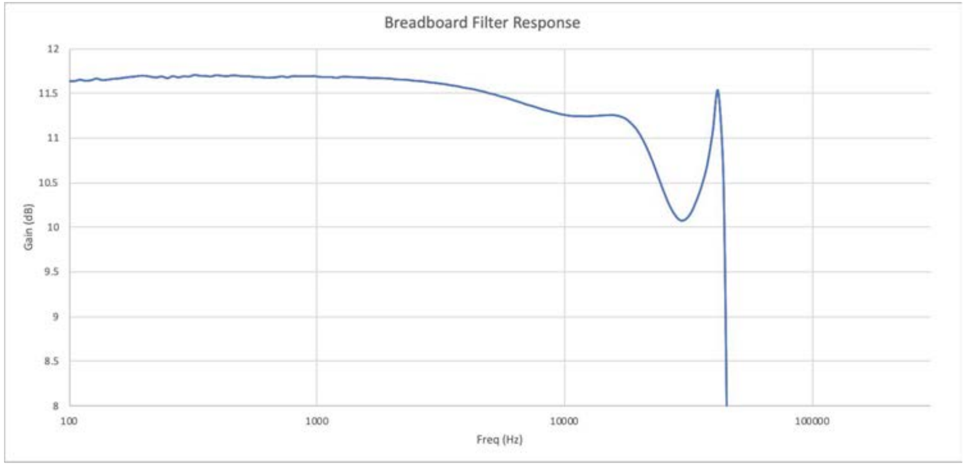
Tuning AAF

update

Move forward



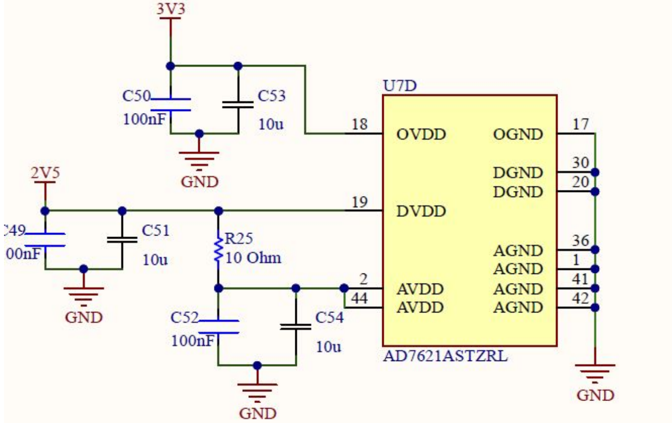
Simulation based on breadboard components and actual tolerances I ordered



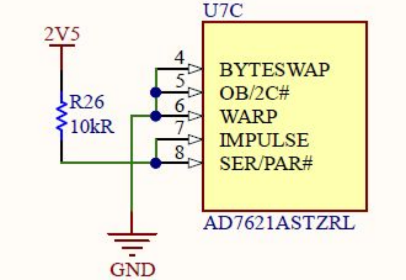
Analog Receiver Board - System Status-ADC

- ADC AD7621
  - 16-bit ADC
  - Based on RAPS design

Power Supply

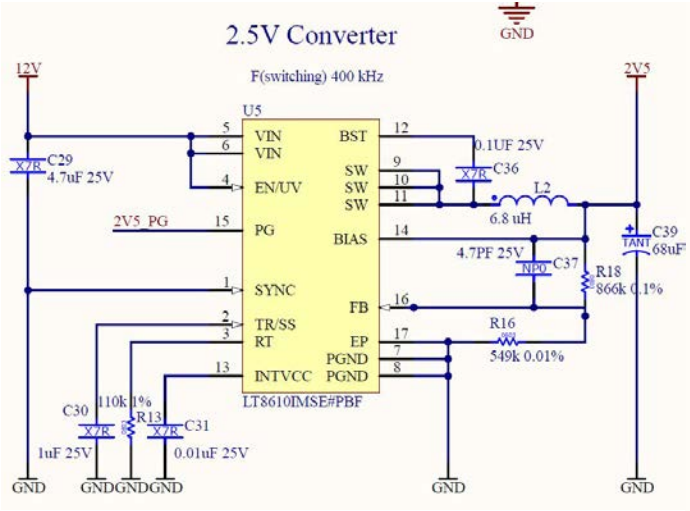


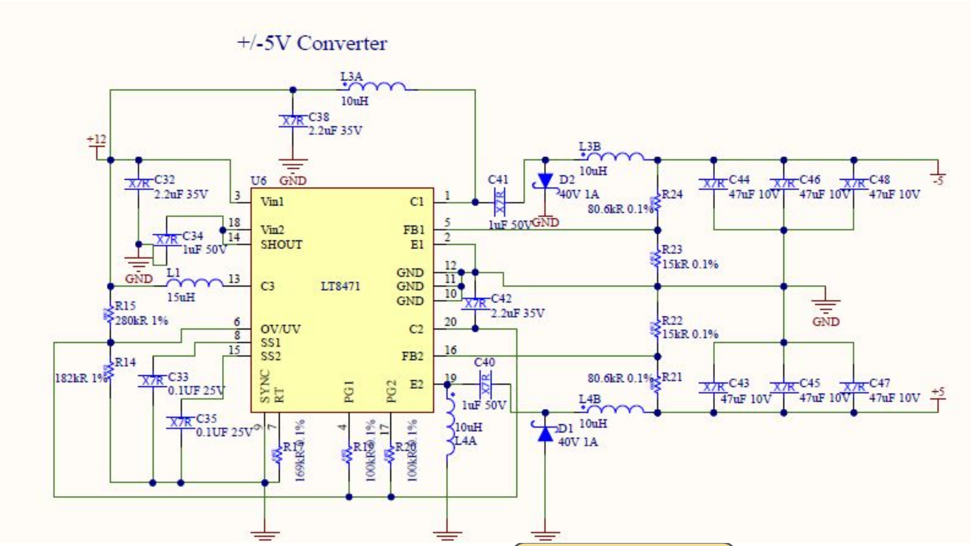
Mode Select



Analog Receiver Board -Status-Power Supply

- Two Converters
  - 12V to 2.5V
  - 12V to +/-5V



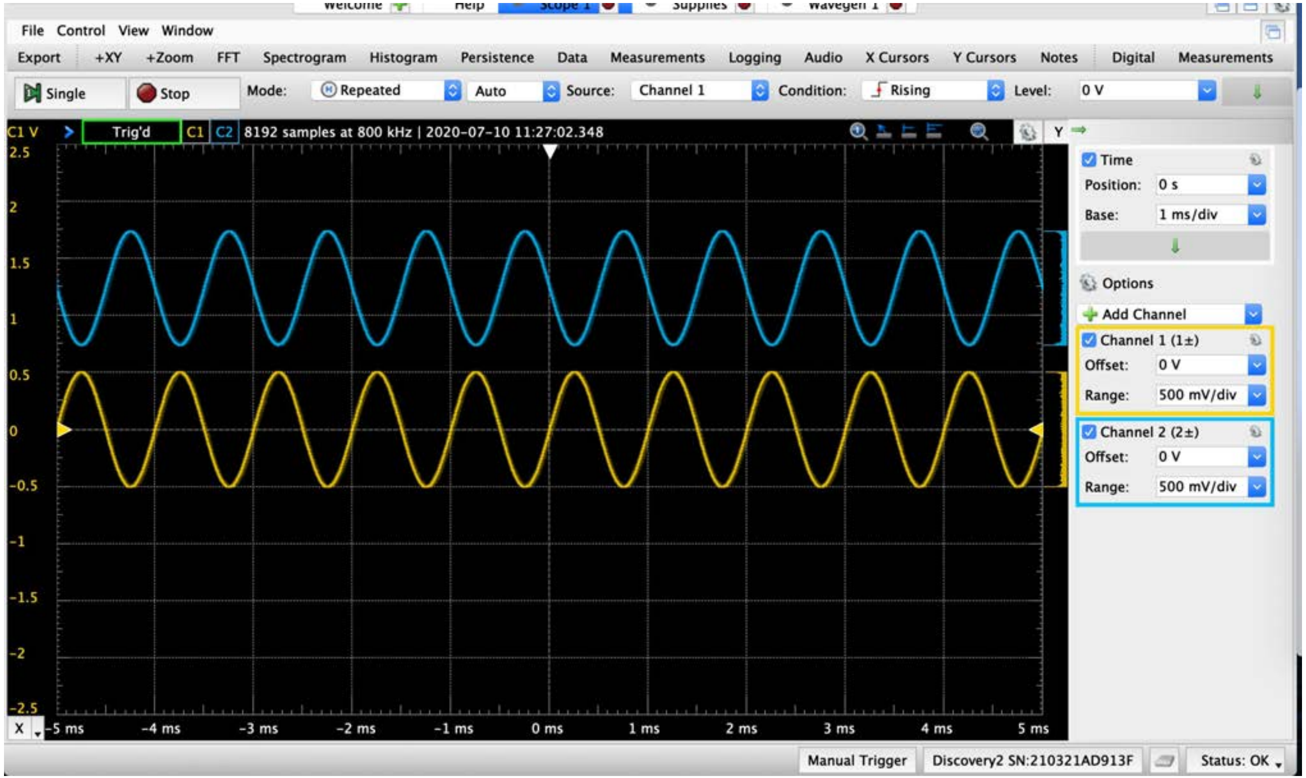


Breadboard level shifter

Breadboard level shifter

update

- Works!
- Was not referencing from signal ground



Instrumentation - Space Rated Passives

NASA Handbook

MIL-HDBK-978B

Also, ->

Research has shown that:

- In general both MIL and space application specifications classify conductive polymer capacitors as not radiation sensitive. Conductive polymer capacitors have been evaluated at total ionization dose (TID) test using a Cobalt 60 source up to 200k rad irradiation at dose rates of 500 rad/hr without impact to the part performance.
- Teflon (PTFE) has demonstrated a rather high susceptibility to radiation damage. Degradation of physical properties occurs when irradiated due to liberated fluorine atoms and the production of entrapped fluorocarbon gases. Tensile strength decreases and the material becomes brittle. Embrittlement becomes severe with extended irradiation [107 rads] and the polytetrafluoroethylene can crumble.
- Ceramic insulating materials show virtually no change in properties (including dielectric constant) with X-ray irradiation to doses of 107 rads and higher.
- When tantalum capacitors are irradiated with ionizing radiation, electrons and holes (positively-charged atoms) are excited into mobile states. The result can be radiation induced discharge in caps with several volts initial bias and radiation-induced voltage buildup across initially unbiased capacitors. Wet tantalum capacitors have been used in space applications for over 40 years, from the early days of the manned space flight programs.
- Electrolytics are general avoided for space applications (although there are mil spec'ed electrolytics available). Electrolytics may undergo parameter changes from either ionizing or burst radiation, depending on dosage. Aluminum electrolytic capacitors can outgas water and organic vapors..The dielectric also can be weakened, and DC leakage may rise as a result of bombardment. NASA found that aluminum capacitors with solid conductive polymer exhibits significant advantages over aluminum capacitors that use a liquid electrolyte.

Recently, AVX's full range of space-level BME X7R dielectric MLCCs – spanning 0603 to 1812 case sizes, 2.2nF to 8.2µF capacitance values, and 16V to 100V ratings – qualified for use in aerospace designs and US military applications under S-311-P-838 for applications including I/O filtering and bulk storage in switch mode power supplies (SMPS) in space and satellite communications and launchers.

Instrumentation - Radiation tolerance of AD7621

43. AD7621

The Linear Technology AD7621 is a 16-bit, 3Msps, charge redistribution Successive Approximation Register, fully differential ADC that operates from a single 2.5 V power supply. It is realized in 0.25µm CMOS technology. The DUTs lot date code was 0501. The AD7621AST was tested for SEL at UCL using the two available cocktails: "High LET" and "High penetration". No SEL events were observed for normal incidence Xe (LET of 55.9MeV-cm²/mg and range of 43µm) and Kr (LET of 32.4 MeV-cm²/mg and range of 92µm) up to a fluence of $1\text{x}10^7$ ions/cm^2[10].

https://trs.jpl.nasa.gov/bitstream/handle/2014/42689/12-3045_A1b.pdf?sequence=1

CDH Radiation Tolerance

Total Ionizing Dose (TID)

- SLC is significantly better than MLC at 20krad (higher density is actually better too!)
  - SLC 32Gb 10^{-7}-10^{-6} % errors
  - MLC 64Gb 10% erros
- Effective Mitigation:
  - ECC for bad block management
  - **Use SLC**
  - Shielding

Single Event Upsets (SEU or SEE)

- SLC is better than MLC (higher density has no measured effect)
  - Slightly less # events
- Effective Mitigation:
  - **ECC for bit errors**
  - Power refresh
  - Redundancy

"[For both TID and SEU] … the complex control circuitry has been demonstrated to be the most vulnerable part of commercial devices"

- https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20140000667.pdf

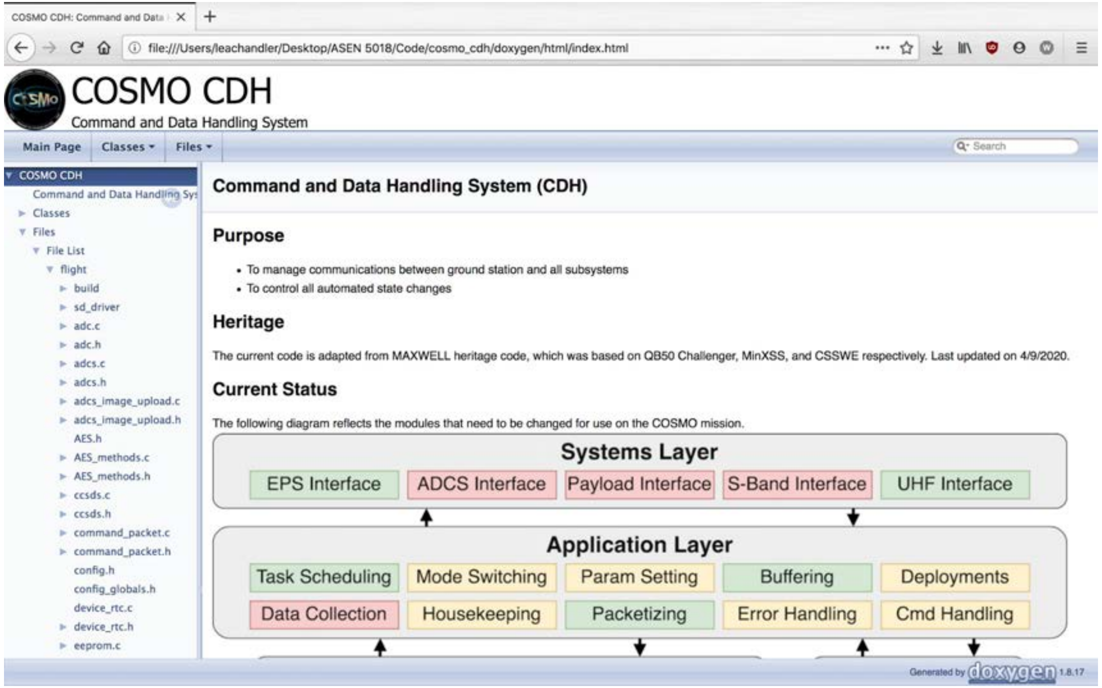
FSW Backup Slides

FSW - Coding Standards

Style	- 4 space indentation - spaces around operators - 80 characters per line - parentheses around conditions - curly brackets for all conditionals
Names	- functions and variables are lowercase with underscores - pins and defines are all uppercase - no difficult abbreviations

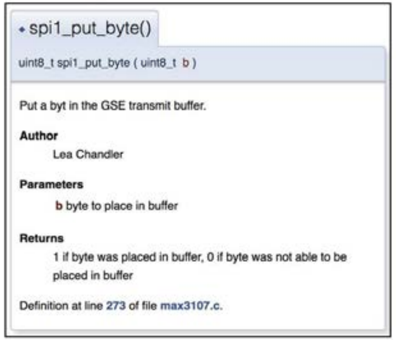
Comments	- Doxygen style comments
	    - Description, author, date, and links for files
	    - Description, inputs, returns for functions
	- TODO comments must have an assignee

FSW - Doxygen




```
/*!
 * @brief Put a byt in the GSE transmit buffer
 * @author Lea Chandler
 * @param b byte to place in buffer
 * @return 1 if byte was placed in buffer, 0 if byte was not able
 *         to be placed in buffer
 */
uint8_t spi1_put_byte(uint8_t b);
```

The resulting documentation looks as follows:



FSW - Task Tracking

No.	Task	Module	Asignee	Status	Date	Comments
8	FSW semester report	-	Lea	In Progress	May 1, 2020	
9	Code introduction document	-	Lea	In Progress	May 4, 2020	
10	Define spacecraft modes and limits	sc_mode.c, sc_mode.h	Lea	In Progress	May 4, 2020	
11	Define S-Band data and registers	hstx.c, hsxt.h	Lea	In Progress	May 4, 2020	
12	Define XACT data, packets, and commands	acds.c, adcs.h	Ryan	In Progress	Spring 2020	
13	CDH pin config	config.h, hw_defines.h	Lea	Not Started	May 15, 2020	
14	S-band downlink task design	hstx.c, hsxt.h	Lea	Not Started	May 22, 2020	

CDH FSW Notes and TODOs

Table of Contents

adc.c/h

- CHANGE: log_adcs() to log_adc() in adc.h
- used in sensors.c
- configures board through variables in the processor header
- samples CDH 5V and battery voltage (directly connected to CDH board) during sensors task
- COSMO/CANVAS: what's connected to the ADCs on the CDH board?

FSW - V&V Resources

config_globals.h

```
/********* Defines just for testing *******/
//#define LOG_STRING_ON_HK_BEACON //For: testing beacon slowdown code (globalstar)
//#define COUNT_UART3_BYTES //Counts incoming uart3 bytes and prints them every time ADCS gets a
//#define ADCS_OPCODE_RX_PRINT //prints out received opcodes
//#define ADCS_PARTIAL_READ_DEBUG_PRINTS //prints out a bunch of stuff during partial reads
//#define ADCS_TEST_DATA_DUMP //testing for ADCS test data dump
//#define GLOBALSTAR_PRINT_SENT_PACKETS //prints out the bytes of each globalstar packet sent (us
//#define LOG_CALLSIGN_BYTES_ON_COMMANDS //prints out a bunch of bytes every time a command is re
//#define TEST_LOG_EVENT_OVERRUN //purposely sends too many bytes to the log_event to test it bre
// #define TEST_ADCS_IMAGE_UPLOAD //prints out messages during ADCS image uploads (log_string)
//#define TEST_FORCE_9600_BAUD //prints out some messages related to the feature to artificially
//#define PRINT_COMMAND_PACKET_EXECUTE_BYTES //prints out every command we get from the ground, f
//#define MAKE_IMAGE_XSUM_VALID //tells the CDH that the ADCS image checksum is always valid (use
//#define SOC_RAMP_TESTING //fakes the SOC ramping up/down from 0-100
#define PRINT_SOC //prints out the state of charge every 30 seconds
// #define TEST_RADIO_TEMP //test the radio temperature safety mechanism (prints out debug info)
//#define DEBUG_SD_DOWNLINK //prints out SD contents when a packet APID doesn't match
#define TEST_RADIO_CONFIG // call test_radio_config() to cycle through testing Li-1 fcns
```

```
#ifdef TEST_RADIO_CONFIG
#include "li1_test.h"
#endif
```

```
#ifdef TEST_RADIO_CONFIG
        test_radio_config();
        test_task_fcn_called = 1;
#endif
```

FSW - Packet Opcodes

XACT
Packet: CCSDS
Opcodes:
- Goto Sunpoint (XACT→CDH)
- Goto MagPoint (XACT→CDH)
- Goto GS (XACT→CDH)
- Telemetry (XACT→CDH)

UHF
Packet: CDI
Opcodes:
- noop (CDH←→UHF)
- reset (CDH→UHF)
- transmit (CDH→UHF)
- data (UHF→CDH)
- get config (CDH←→UHF)
- set config (CDH→UHF)
- telemetry (CDH←→UHF)
- write flash (CDH→UHF)
- rf config (CDH→UHF)
- beacon data (CDH→UHF)
- beacon config (CDH→UHF)
- read firmware (CDH←→UHF)

Payload
Packet: **TBD**
Opcodes: **TBD**

EPS
Packet: **TBD**
Opcodes:
- get hk (EPS←→CDH)

Downlink
Packet: CCSDS
Opcode:
- Command echo
- Housekeeping
- Beacon
- Param Dump
- Event Log
- Science Data

Commands
Packet: CCSDS
Opcodes:
- noop
- reset counters
- set time
- copy params
- dump params
- upload params
- set mode
- echo enable
- realtime HK
- event log route
- playback telem range
- start playback
- set ground contact timeout
- component power
- deply antenna
- deploy solar arrays
- set heater
- write to cdh mem
- read from cdh mem
- write to eeprom
- radio cmd
- get radio config
- enable dual cmd
- tx toggle
- set radio amp
- trigger wdt reset
- send adcs cmd
- get adcs config
- send hstx cmd
- get hstx config
- set next pass

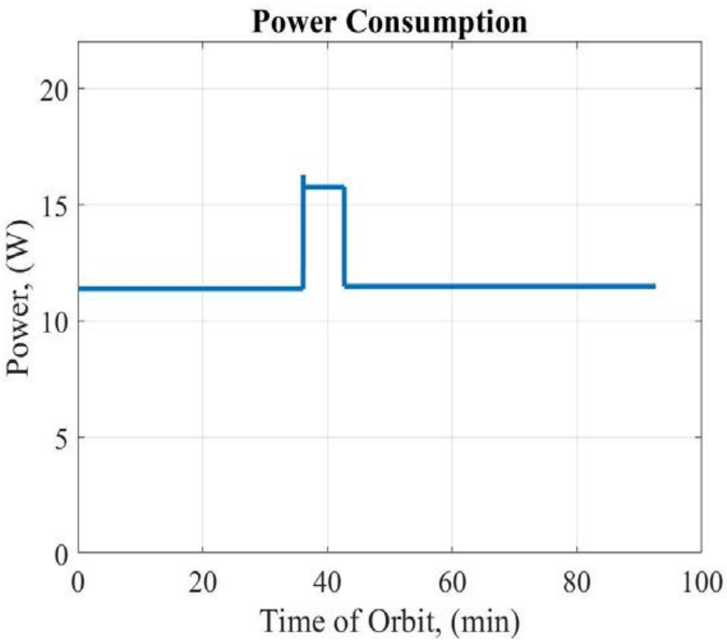
EPS Backup Slides

Battery Capacity Analysis and Design

Energy drained from batteries over orbit

- 8.85 Whr
- Factor in SOC
- Capacity Requirement: 22.12 Whr EOL
- 20% assumed battery degradation
- Capacity: 76.96 Whr BOL
- Capacity: 61.57 Whr EOL

Design: 2 Tenergy batteries
Margin: **178%**



Solar Panel Design

AZUR Space Solar Cells

- EOL eff of 26.6%
- 3.56 g/cell
- 30.18 cm^2/cell

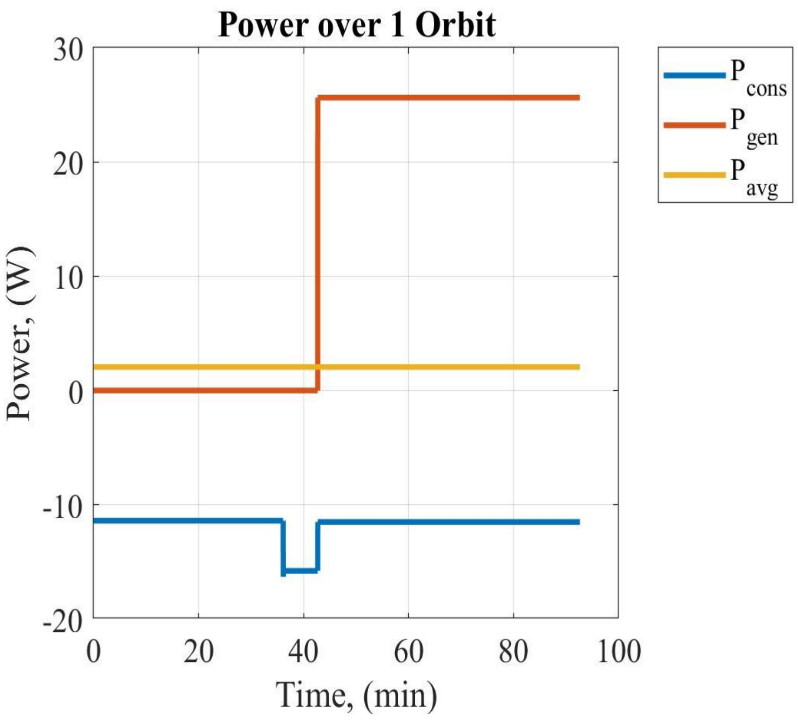
Assuming:

- PPT 90%
- Max offpoint 15 deg

Power Generation Requirement: 22.54 W

Design # of cells: 27 (25.63 W, EOL)

Margin: **14%**

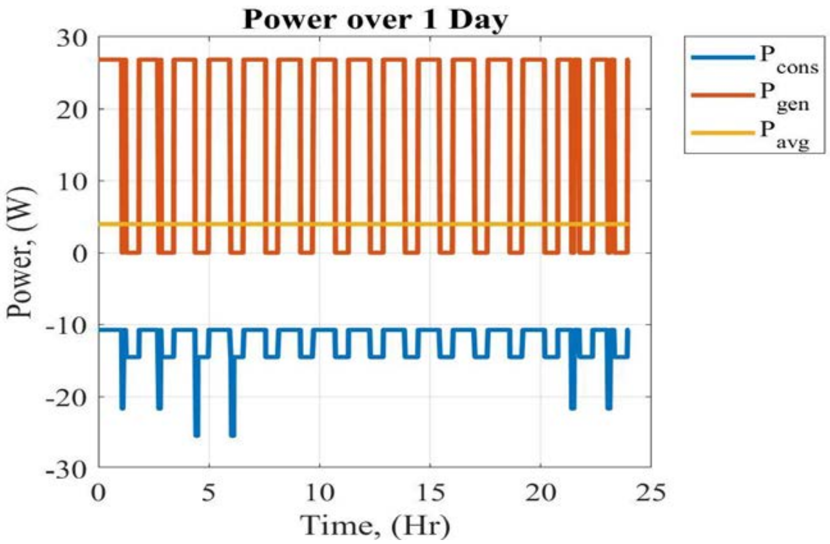


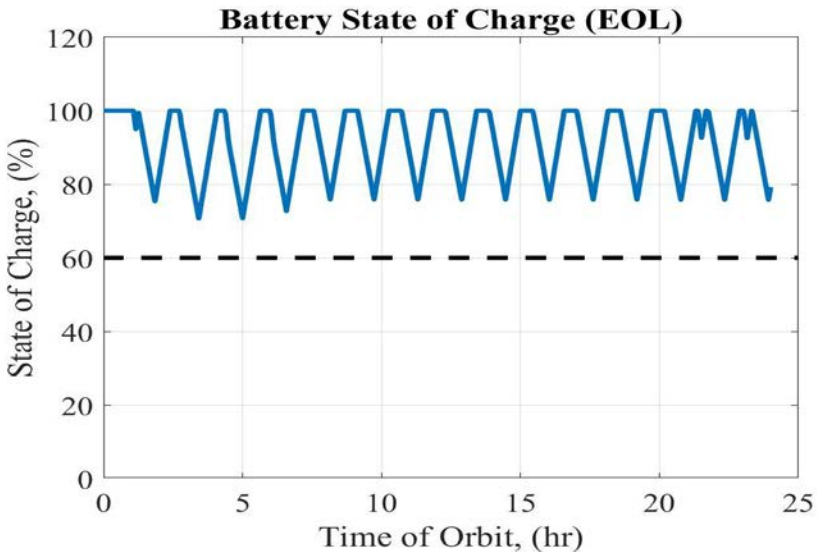
Day in the Life

Battery Design: 2 Tenergy Li-Ion 18650, 61.57 Whr (EOL)

Solar Panel Design: 27 Azur Space cells, 25.63 W (EOL)

- Since minimum state of charge is larger than 60% the EPS batteries meet **KDR EPS - 2.1**, The subsystem battery shall not fall below a depth of discharge of 60%
- Since subsystem remains power positive it meets **KDR EPS - 1**, The subsystem shall be power positive on average over the course of an orbit

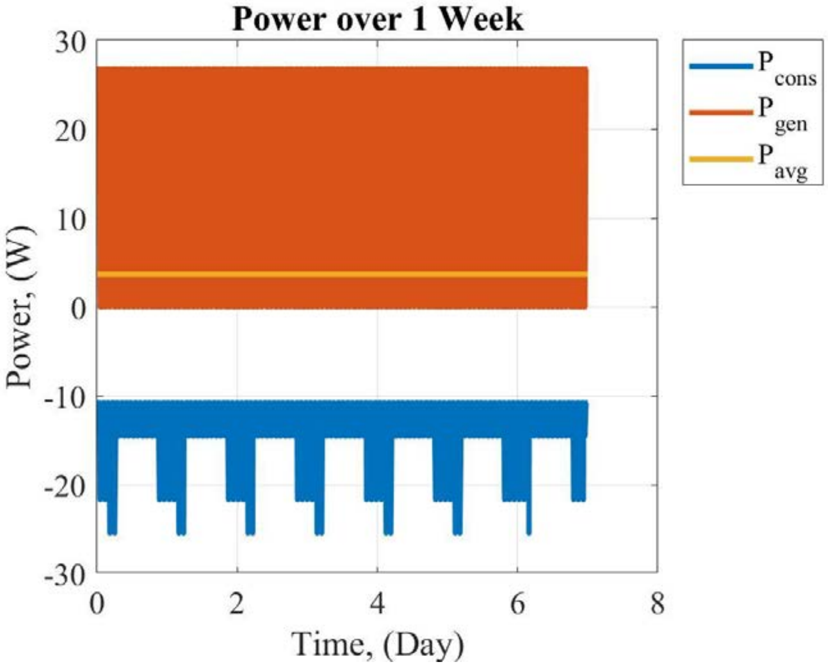


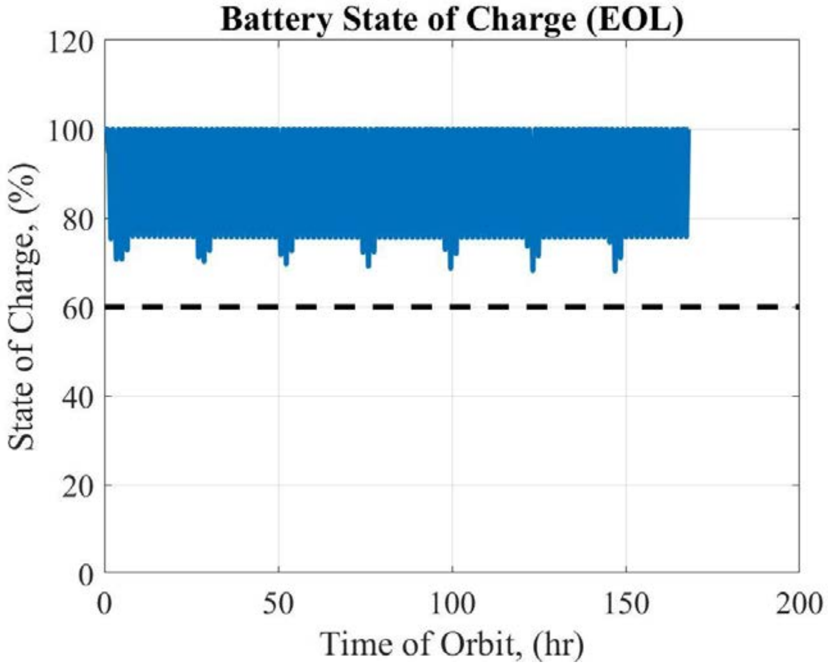


Day in the Life

Battery Design: 2 Tenergy cells, 61.57 Whr (EOL)

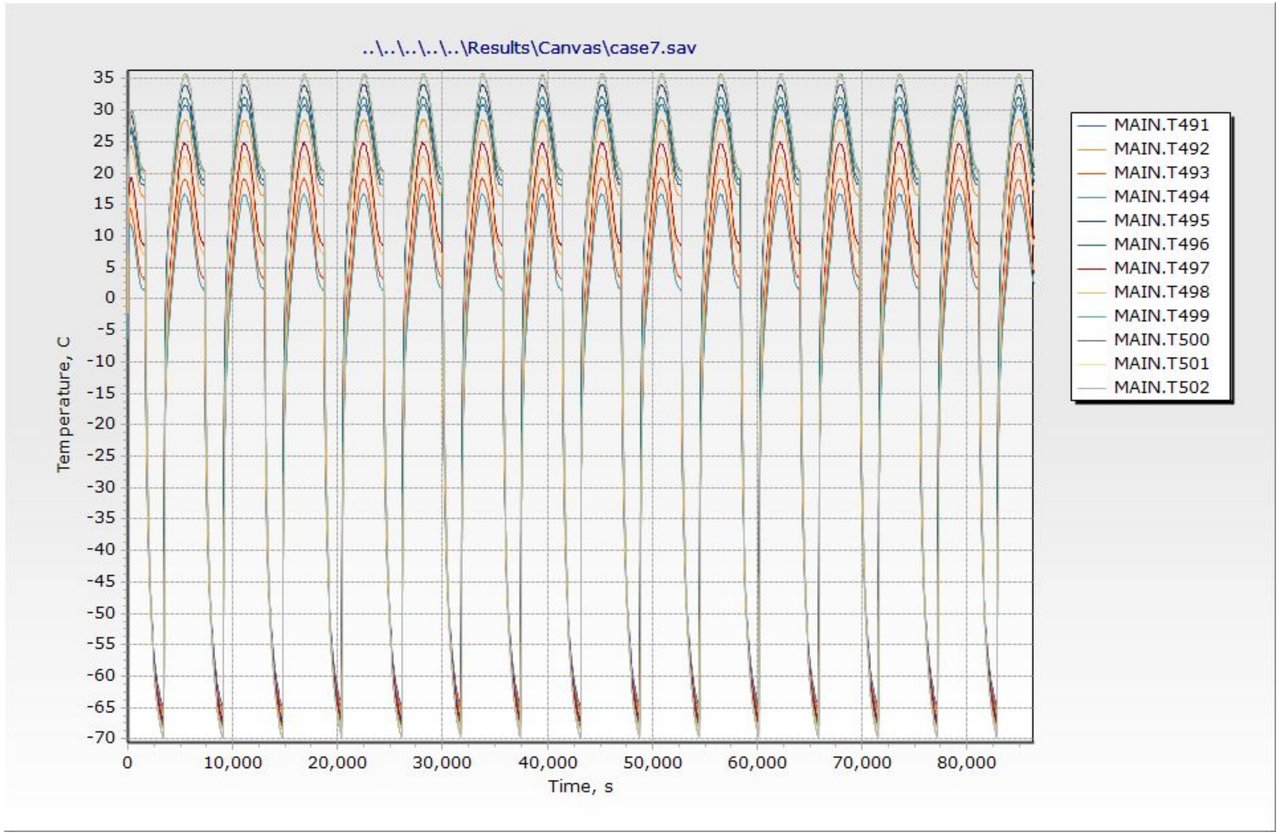
Solar Panel Design: 27 Azur Space cells, 25.63 W (EOL)



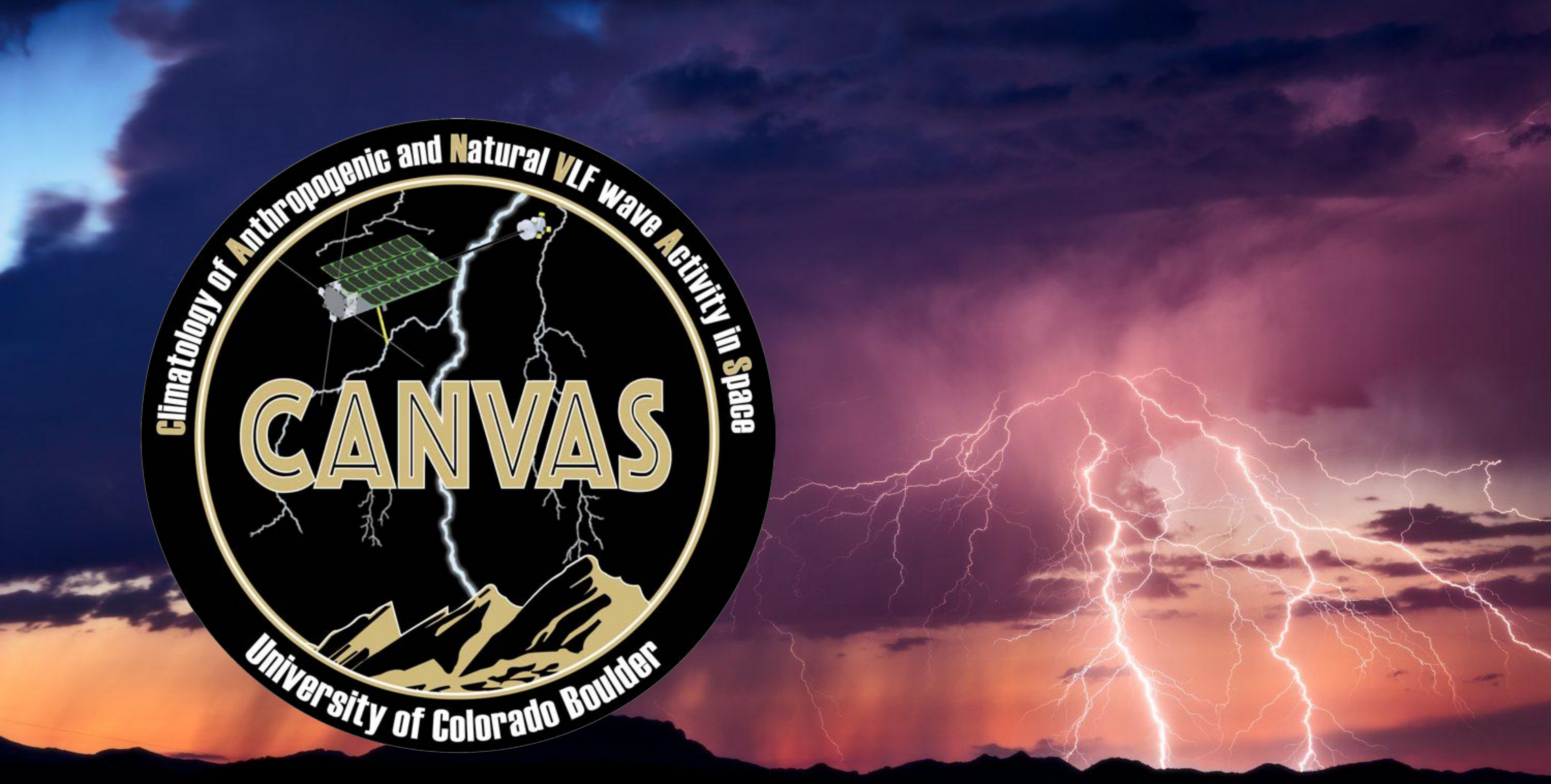


Thermal Backup Slide

Efield Antenna Delrin Piece - w/black coated Antenna



** Delrin melting point ~ 150C*


Climatology of Anthropogenic and Natural VLF wave Activity in Space
CANVAS
University of Colorado Boulder