SOIMUMPs Design Handbook

a MUMPs® process

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MEMSCAP

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Chapter 1
Silicon on Insulator (SOI) Micromachining Process

1.1 Introduction

The Multi-User MEMS Processes, or MUMPs®, is a commercial program that provides cost-effective, proof-of-concept MEMS fabrication to industry, universities, and government worldwide. MEMSCAP offers three standard processes as part of the MUMPs® program: **PolyMUMPs**, a three-layer polysilicon surface micromachining process: **MetalMUMPs**, an electroplated nickel process; and **SOIMUMPs**, a silicon-on-insulator micromachining process.

The following is a general process description and user guide for SOIMUMPs, which is designed for general-purpose micromachining of Silicon-on-Insulator (SOI) structures. Chapter 1 of this document explains the process step-by-step, while Chapter 2 outlines the design rules for the process.

Though this document is geared toward designers who do not have a strong background in microfabrication, it contains information that is useful to all MUMPs® users. Regardless of the level of the designer, we strongly recommend all users of SOIMUMPs review this document prior to submitting a design.

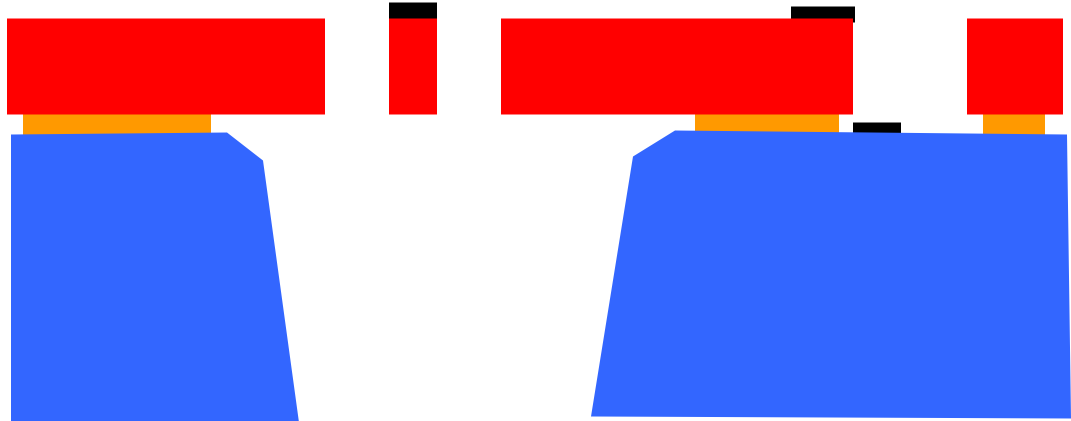


FIGURE 1.1. Cross sectional view showing all layers of the SOI-MUMPs process (not to scale).

Figure 1.1 is a cross section of the silicon-on-insulator micromachining SOIMUMPs process. This process has the following general features:

1. A silicon-on-insulator (SOI) wafer is used as the starting substrate. This wafer has the following layer thicknesses:
    - Silicon thickness: 10 ± 1 µm
    - Oxide thickness: 1 ± 0.05 µm
    - Handle wafer (Substrate) thickness: 400 ± 5 µm
2. The Silicon layer is doped and patterned and etched down to the Oxide layer. This layer can be used for mechanical structures, resistor structures, and/or electrical routing.
3. The Substrate can be patterned and etched from the “bottom” side to the Oxide layer. This allows for through-hole structures.
4. A shadow-masked metal process is used to provide coarse Metal features such as bond pads, electrical routing, and optical mirror surfaces.
5. A second pad-metal feature that allows finer metal features and precision alignment but limited to areas not etched in the silicon device layer.

The process is designed to be as general as possible, and to be capable of supporting many different designs on a single silicon wafer. Since the process was not optimized with the purpose of fabricating any one specific device, the thickness of the layers were chosen to suit most users, and the design rules were chosen conservatively to guarantee the highest yield possible.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

1.2 Process Overview

The SOIMUMPs process is a simple 4-mask level SOI patterning and etching process derived from work performed at MEMSCAP (formerly Cronos Integrated Microsystems and the MCNC MEMS Technology Applications Center). A version of this process flow was originally developed for the fabrication of MEMS variable optical attenuator (VOA) devices based on a patented thermal actuator technology. The process flow described below is designed to introduce users to this micromachining process. The text is supplemented by drawings that show the process flow in the context of building a patented thermal actuator.

The process begins with 100 mm n-type double-side polished silicon on insulator wafers. These wafers consist of a 10µm Silicon layer, a 1µm Oxide layer, and a 400µm Substrate layer. A Bottom Side Oxide layer that is slightly thinner than the Oxide layer is also present on the bottom side of the Substrate layer (Figure 1.2). The top surface of the Silicon layer is doped by depositing a phosphosilicate glass (PSG) layer and annealing at 1050°C for 1 hour in Argon (Figure 1.3). This PSG layer is then removed via wet chemical etching.

The first layer in the process is the pad metal. A metal stack of 20 nm of chrome and 500 nm of gold is patterned through a liftoff process. 3 µm lines with 3 µm space features may be patterned with a 3 µm alignment tolerance to the device layer. This metal area must be covered during the subsequent DRIE etch. Hence, it is limited to relatively large areas in the actuator. Because this metal is exposed to high temperature during the subsequent process, surface roughness tends to be higher and not suitable for low-loss optical mirror applications.

Silicon is lithographically patterned with the second mask level, SOI, and deep reactive ion etched (DRIE) (Figure 1.5). This etch is performed using inductively coupled plasma (ICP) technology, and a special SOI recipe is used to virtually eliminate any undercutting of the Silicon layer when the etch reaches the Oxide.

Next, a frontside protection material is applied to the top surface of the Silicon layer. The wafers are then reversed, and the Substrate layer is lithographically patterned from the bottom side using the third mask level, TRENCH. This pattern is then reactive ion etched (RIE) into the Bottom Side Oxide layer. A DRIE silicon etch is subsequently used to etch these features completely through the Substrate layer. A wet oxide etch process is then used to remove the Oxide layer in the regions defined by the TRENCH mask (Figure 1.6). The frontside protection material is then stripped in a dry etch process. This "releases" any mechanical structures in the Silicon layer that are located over through-holes defined in the Substrate layer. The remaining "exposed" Oxide layer is removed from the wafers using a vapor HF process to minimize stiction. The exposed Oxide layer is removed to allow for electrical contact to the Substrate and to provide an undercut in the oxide layer that will prevent metal shorts between the Silicon layer and the Substrate layer. (Figure 1.7)

The Blanket Metal layer, consisting of 50nm Cr+ 600nm Au, is deposited and patterned using a shadow masking technique. The shadow mask is prepared from a separate double side polished silicon wafer. "Standoffs" are incorporated into the side of the shadow mask that will contact the SOI wafer, to avoid any contact with patterned features in the Silicon layer. The shadow mask is then patterned with the METAL mask, and through holes are DRIE etched (Figure 1.8). The shadow mask is then aligned and temporarily bonded to the SOI wafer, and the Metal is e-beam evaporated. Metal is deposited on the top surface of the Silicon layer only in the through hole regions of the shadow mask (Figure 1.9). After evaporation, the shadow mask is removed, leaving a patterned Metal layer on the SOI wafer (Figure 1.10).

The wafers are then diced using a scribe and break method, sorted and shipped to the SOIMUMPs user.

The following pages provide a graphical representation of the process steps.

Starting Substrate - SOI Wafer

FIGURE 1.2. The SOI wafers consist of a 10µm Silicon layer, a 1µm Oxide layer, and a 400µm Substrate layer. A Bottom Side Oxide layer is also initially present on the wafers.

Silicon Doping

FIGURE 1.3. A phosphosilicate glass layer (PSG) is deposited, and the wafers are annealed at 1050°C for 1 hour in Argon to drive the Phosphorous dopant into the top surface of the Silicon layer. The PSG layer is subsequently removed using wet chemical etching.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

Metal Liftoff **Mask Level: Pad Metal**

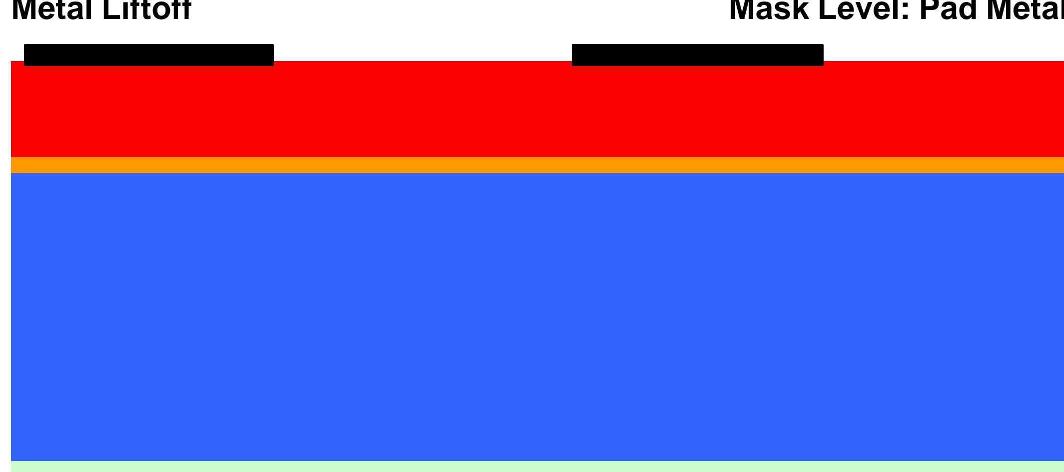


FIGURE 1.4. The wafers are coated with negative photoresist and lithographically patterned by exposing the photoresist with light through the first level mask (Pad MET), and then developing it. A metal stack consisting of 20 nm chrome and 500 nm gold is deposited over the photoresist pattern by e-beam evaporation. The photoresist is then dissolved to leave behind metal in the opened areas.

Silicon Patterning **Mask Level: SOI**

FIGURE 1.5. The wafers are coated with UV-sensitive photoresist and lithographically patterned by exposing the photoresist to UV light through the first level mask (SOI), and then developing it. The photoresist in exposed areas is removed, leaving behind a patterned photoresist mask for etching. Deep reactive ion etching (DRIE) is used etch the Silicon down to the Oxide layer. After etching, the photoresist is chemically stripped.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

Substrate Patterning — Mask Level: TRENCH

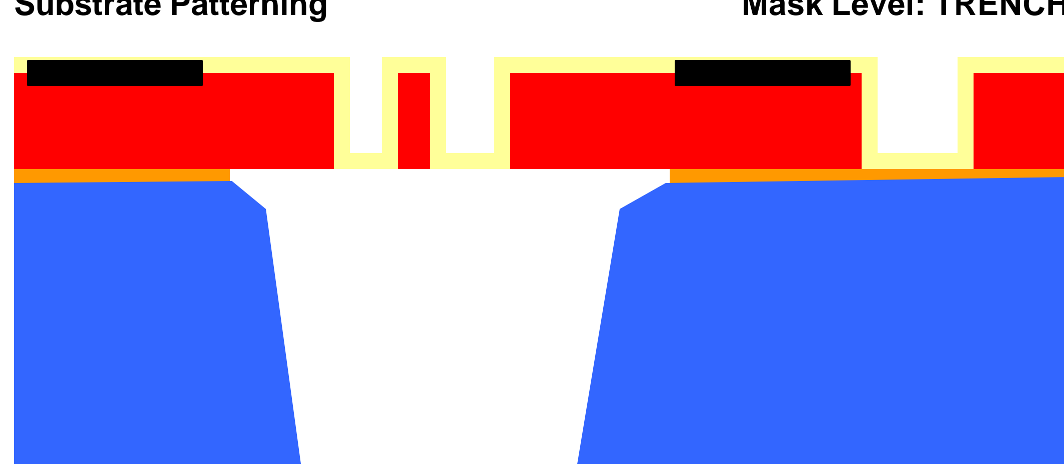


FIGURE 1.6. A frontside protection material is applied to the top surface of the patterned Silicon layer. The bottom side of the wafers are coated with photoresist and the second level (TRENCH) is lithographically patterned. Reactive ion etching (RIE) is used to remove the Bottom Side Oxide layer. A DRIE silicon etch is subsequently used to etch completely through the Substrate layer, stopping on the Oxide layer. After the etch is completed, the photoresist is removed. A wet oxide etch process is then used to remove the Oxide layer in the regions defined by the TRENCH mask.

“Release”– Protection layer and Oxide layer removal

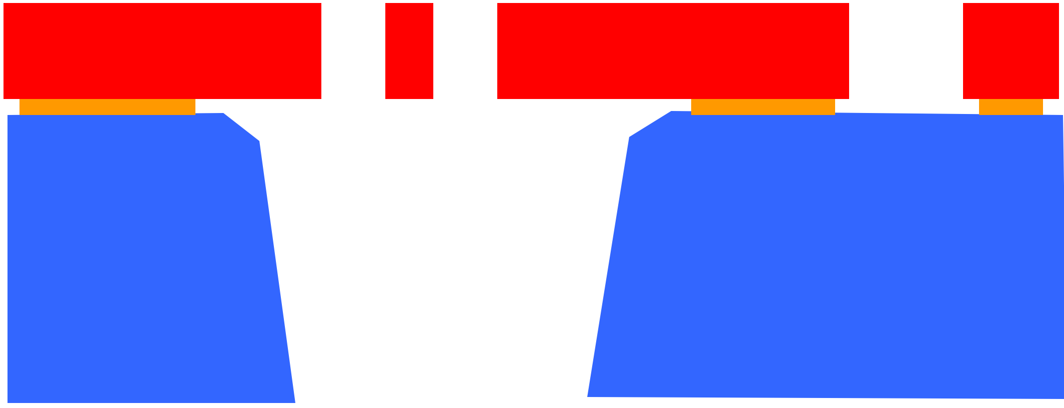


FIGURE 1.7. The frontside protection material is then stripped using a dry etch process. The remaining “exposed” Oxide layer is removed from the top surface using a vapor HF process. This allows for an electrical contact to the Substrate layer, and provides an undercut of the Oxide layer.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

Metal Shadow Mask Fabrication — Mask Level: Blanket METAL

FIGURE 1.8. A separate silicon wafer is used to fabricate a shadow mask for the Metal pattern. Standoffs are prefabricated into the shadow mask so that the shadow mask does not come into contact with patterned features in the Silicon layer of the SOI wafer. The shadow mask wafers are then coated with photoresist and the fourth level (METAL) is lithographically patterned. DRIE silicon etching is used to etch completely through the shadow mask wafer, producing through holes for the Metal to be evaporated. After the etch is completed, the photoresist is removed

Shadow Mask Bonding and Metal Deposition

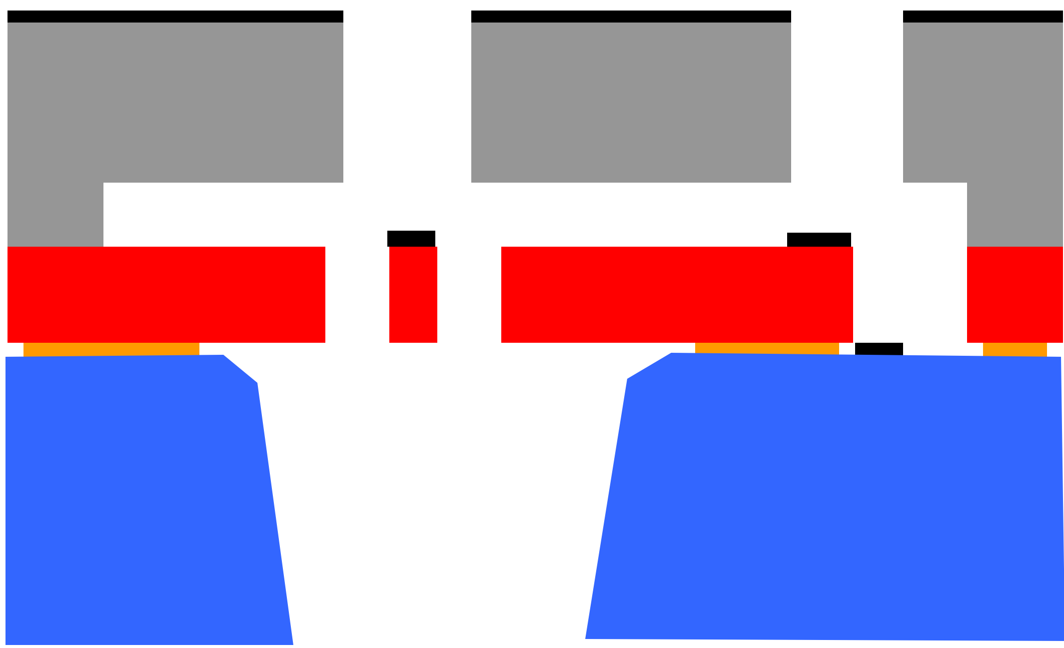


FIGURE 1.9. The shadow mask is aligned and temporarily bonded to the SOI wafer. The Metal layer, consisting of 50nm Cr + 600nm Au, is deposited through the shadow mask.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

Shadow Mask Removal

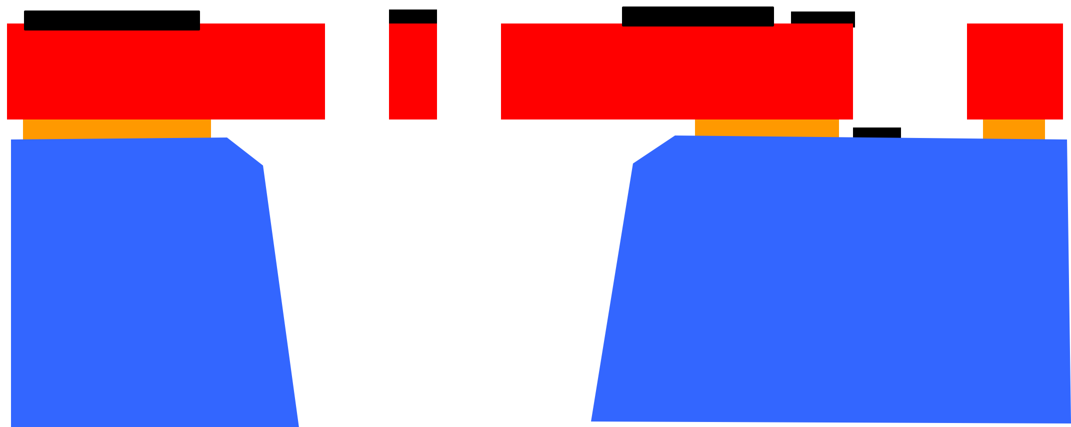


FIGURE 1.10. The shadow mask is removed, leaving a patterned Metal layer on the SOI wafer.

	Silicon		**Substrate**		**Bottom Oxide**		**Shadow Mask**
	Oxide		**Metal**		**PSG (dopant)**		**Frontside Protection Material**

Chapter 2
SOIMUMPs Design Rules and Considerations

2.1 Introduction

The purpose of the design rules is to ensure the greatest possibility of successful fabrication. The rules have evolved through process development and the experience of the MEMSCAP staff. The design rules are a set of requirements that are defined by the limits of the process (i.e. the stable process window) that in turn are defined by the capabilities of the individual process steps. In general, minimum design rules are defined by the resolution and alignment capabilities of the lithography and resolution and uniformity of the etching systems. This section of the document describes the design rules that exist for the SOIMUMPs micromachining process.

Design rules in the document define the minimum feature sizes and spaces for all levels and overlay accuracies between relevant levels. The **minimum line widths and spaces are mandatory rules**. Mandatory rules are given to ensure that all layouts will remain compatible with MEMSCAP MEMS' lithographic and etch process tolerances. Violation of minimum line/space rules will result in missing, undersized, oversized or fused features. **Please note: The minimum geometry allowed should not be confused with the nominal geometry a designer uses. Minimum geometries should only be used where absolutely necessary.** When size is not an issue, the feature should be designed larger than the minimum allowed value.

Finally, there are a few things to keep in mind regarding naming conventions. Lithography levels (i.e. names for each masking level) will be written in upper case. When referring to a specific layer of material the material will be typed in lower case with the first letter capitalized. For example SOI refers to the masking level for patterning the Silicon layer (Silicon). Table 2.1 outlines the material layer names, thicknesses and the lithography levels associated with those layers.

Material Layer	Thickness (μm)	Lithography Level Name	Lithography Level Purpose	Comments
Pad Metal	0.52	PADMETAL	Provide metal for electrical interconnects	20 nm Cr 500 nm Au
Silicon	10.0	SOI	Define structures in Silicon layer of SOI wafer	
Oxide	1.0			
Substrate	400	TRENCH	Define through-hole structures in Substrate layer of SOI wafer	
Blanket Metal	0.65	BLANKETMETAL	Pattern through holes in shadow mask. The shadow mask is then bonded to the SOI wafer so that a patterned Metal layer is achieved when the Metal is deposited.	50nm Cr + 600nm Au

TABLE 2.1. Layer names, thicknesses and lithography levels

2.2 Design Rules

Table 2.2 lists the cross-reference between the MEMSCAP descriptive name, the CIF name and the GDS level number. These are the level names and numbers referred to in the process guide and in any communications you may have with MEMSCAP MEMS' layout support. Please adopt this naming scheme on your own layout system to minimize confusion when you transfer your data file to MEMSCAP for fabrication. The table also lists the associated design rules for that level. These are mandatory rules. Explanations for these rules are discussed in the following sections.

Mnemonic level name	CIF level name	GDS level number	Min. feature (μm)	Min. space (μm)	Max. feature length (μm)	Max. patterned (etched) area
PADMETAL	PMETL	5	3	3	5000	20 mm^2
SOI	SOI	10	2*	2*	Unlimited for width >6μm (See section 2.2.1)	33 mm^2
TRENCH	TRCH	20	200	200	5000	20 mm^2
BLANKETMETAL	BMETL	30	100	100	5000	20 mm^2

TABLE 2.2. MEMSCAP level name, CIF and GDSII™ level designation, and associated design rules. See following sections for explanation of design rules.

It should be noted that the photo masking process used by MEMSCAP is capable of rendering arcs and non-rectangular polygons. You are welcome and encouraged to include non-Manhattan geometries as part of your submission. Keep in mind, however, that the masks are printed with a 0.25 μm spot size and all features are limited by this registration. To minimize vertex snapping errors in the fracturing of the data, please use a 0.25 micron grid in layout and avoid rotating cells.

*Due to pixelation of the 0.25 um resolution photomasks, features and spaces that are drawn on non-orthogonal axes may not print on the wafer at the nominal sizes. In the case of closely spaced SOI features, this can lead to bridging between the features or abnormally small spaces. *To minimize the possibility of bridging, it is recommended that for non-orthogonal features, designers default to a 3 mm nominal line/space rule for the SOI level rather than the 2 mm minimum values.*

2.2.1 Maximum Feature Length – SOI Level

Table 2.2 indicates that there is no maximum length for features patterned using the SOI layer, as long as those features have a width that is greater than 6μm. Silicon features patterned using the SOI layer that are less than 6μm may be "released" from the Substrate due to the undercutting of the Oxide layer during the HF vapor removal of the exposed Oxide regions. ***(See section 2.4.2 "Silicon Layer Release and Anchor).***

"Long" released Silicon structures have a tendency to curl out of plane due to the intrinsic stresses in the Silicon layer, and the surface stress caused by the doping process. The amount of out-of-plane distortion will depend on the length and design of the released structures. For example, 2μm Silicon beams that are anchored at one end will curl out-of-plane to a greater degree than 2μm Silicon beams that are anchored at both ends. *To minimize these effects, an initial conservative guideline for SOI patterns that are less than 6μm in width, is to use a maximum length of 100μm if the structure is anchored at one end only and 500μm if the structure is anchored at two (or more) ends.* MEMSCAP will continue to analyze this effect, and will update these guidelines as additional data is collected.

2.2.2 Maximum Feature Length – TRENCH and METAL Levels

The maximum feature length rule in Table 2.2 for the TRENCH and both METAL levels is intended to ensure the sturdiness of the SOI wafer and Shadow Mask wafer substrates following the DRIE etching processes. Features longer than the maximum values could compromise the mechanical integrity of the substrates, leading to chip or wafer breakage.

2.2.3 Maximum Patterned Area

The uniformity of the DRIE etching processes are strongly dependent upon feature size and the amount of silicon area that is etched. In order to minimize non-uniformities, and to ensure that the pattern from one chip design does not influence the etch results of a neighboring chip design, we require that the total area of silicon that is etched (as defined by the relevant mask pattern) be constrained as follows:

SOI Mask Layer:	*Area of Silicon etched < 33mm^2 (33% of Chip Area)*
TRENCH Mask Layer:	*Area of Substrate etched < 20mm^2 (20% of Chip Area)*
BLANKETMETAL Mask Layer:	*Area of Shadow Mask Silicon etched < 20mm^2 (20% of Chip Area)*

2.3 Level to Level Overlay Rules

In the SOIMUMPs process, both the TRENCH and METAL mask levels are intended for producing coarse features where tight alignment tolerances are not required. In the fabrication process, both the TRENCH and METAL levels are aligned to the SOI mask level. Table 2.3 summarizes the overlay tolerances between these mask levels, and the following sections explain these values.

Layer Combination	Center to Center Overlay Tolerance (μm)	Edge to Edge Bias (μm)
PADMETAL to SOI	±3	± 3
TRENCH to SOI	± 5	< 50
METAL to SOI	± 20	± 25

TABLE 2.3. Level to Level Overlay Rules

2.3.1 PADMETAL to SOI Overlay

Figure 2.3.1 illustrates the PADMETAL to SOI overlay tolerances described in Table 2.3. The "Edge-to-Edge" overlay tolerance accounts for the lithography alignment between the PADMETAL and SOI. PADMETAL must not extend over the SOI edge during DRIE to avoid masking.

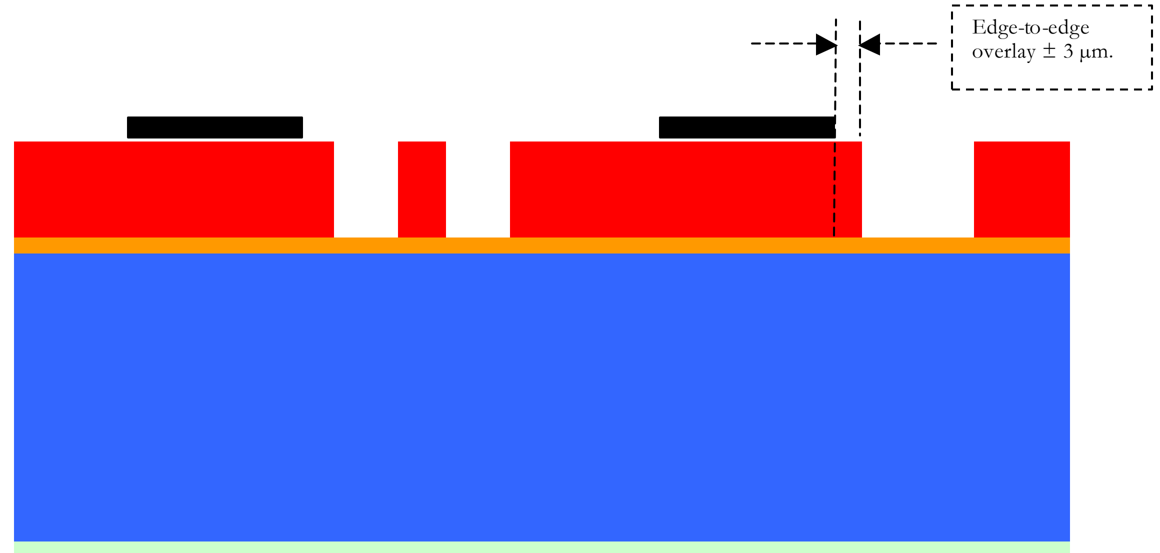


FIGURE 2.3.1. Illustration of the PADMETAL to SOI overlay tolerances given in Table 2.3

2.3.2 TRENCH to SOI Overlay

Figure 2.3.2 illustrates the TRENCH to SOI overlay tolerances described in Table 2.3. The “Center to Center” overlay tolerance accounts for the bottom side to top side lithography alignment between the TRENCH and SOI mask levels. The TRENCH to SOI “Edge to Edge” bias accounts for the etch profile of the through holes in the Substrate layer and the “blow-out” of the etch profile at the Substrate – Oxide interface.

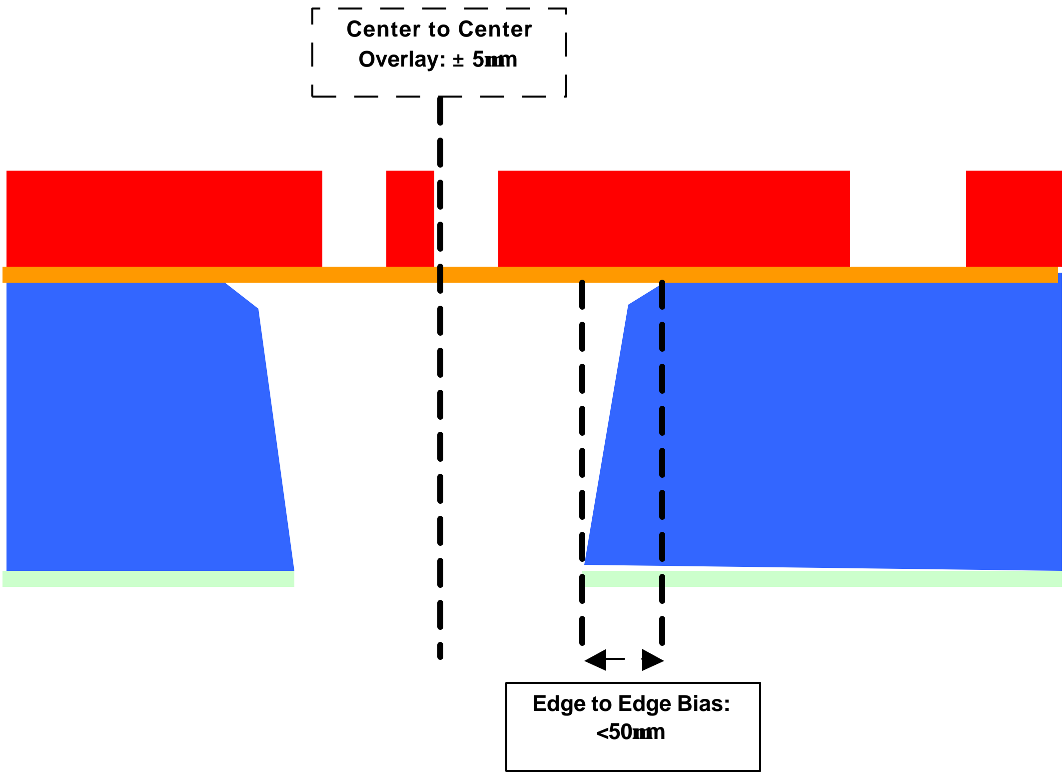


FIGURE 2.3.2. Illustration of the TRENCH to SOI overlay tolerances given in Table 2.3

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

2.3.3 METAL to SOI Overlay

Figure 2.3.3 illustrates the METAL to SOI overlay tolerances described in Table 2.3. The “Center to Center” overlay tolerance accounts for the wafer to wafer bonding alignment between the shadow mask and the SOI wafer. The METAL to SOI “Edge to Edge” bias accounts for the etch profile of the through holes in the Shadow Mask and the dispersion of the Metal layer as it is deposited through the shadow mask onto the SOI wafer.

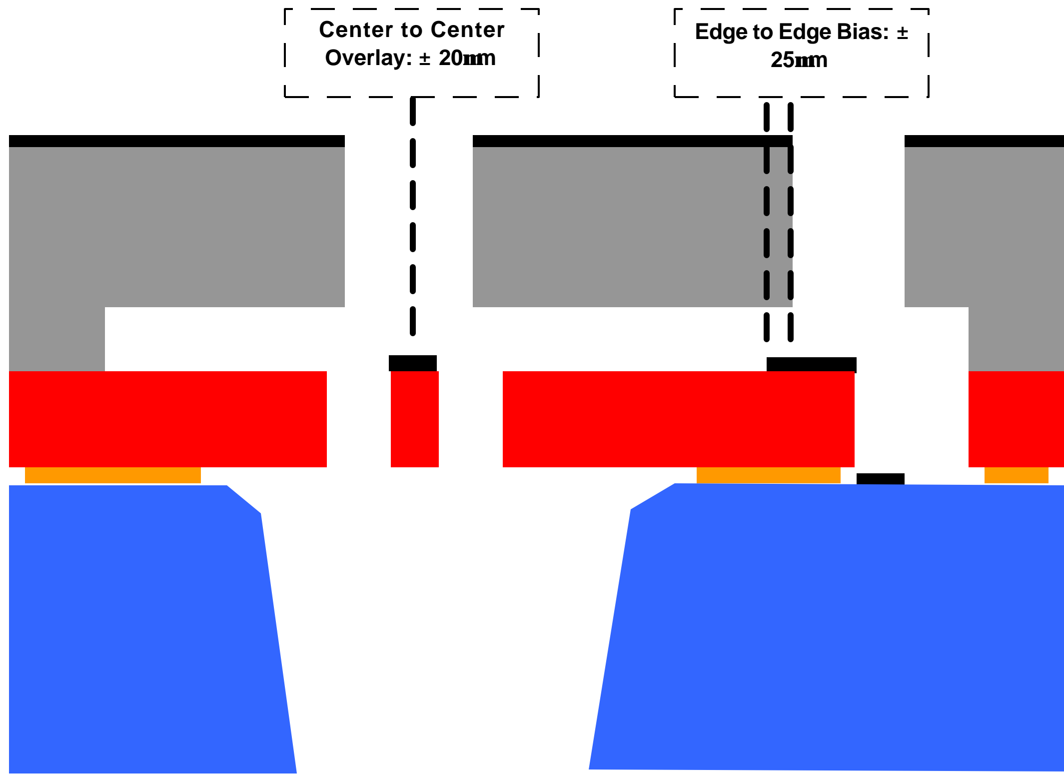


FIGURE 2.3.3. Illustration of the METAL to SOI overlay tolerances given in Table 2.3

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

2.4 Beyond the Design Rules

Section 2.4 is highly recommended reading for any SOIMUMPs user, novice or experienced. It includes information that will optimize your SOIMUMPs design for success, and should prevent several common design errors.

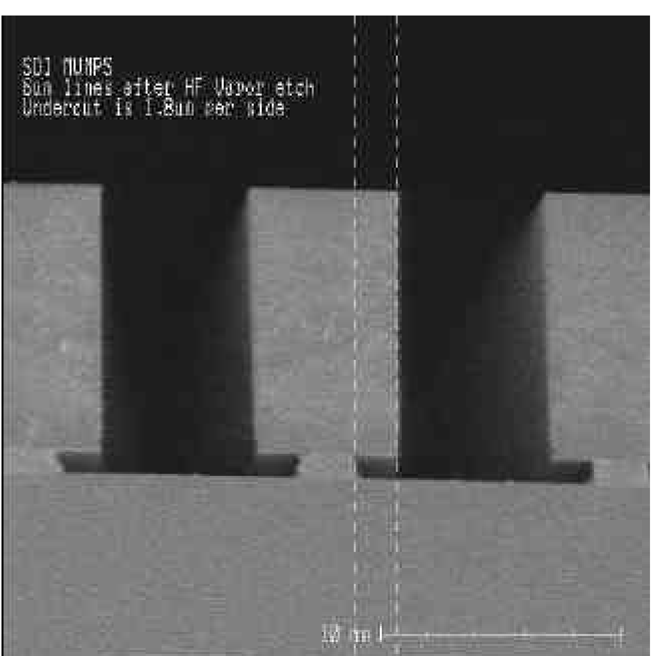
2.4.1 Layout convention

The following convention used by the SOIMUMPs processes in defining mask levels: For the SOI and Pad Metal levels the mask is light field. For this level, draw (i.e. digitize) the feature you want to keep. The TRENCH and Blanket Metal levels are dark field. For the Trench, draw the trench you want to etch and for the Blanket Metal, draw where you want Metal. It is imperative that these conventions be followed for your devices to be fabricated correctly.

2.4.2 Silicon Layer Release and Anchor

In the MUMPs SOI process, the "release" of structures in the Silicon layer is accomplished by placing the structures to be released over a TRENCH feature in the substrate. Following the DRIE etch to remove the Substrate in the TRENCH features, the Oxide layer is wet-etched, thus freeing any structures in the Silicon layer that are placed over the TRENCH. The protective material is then removed from the frontside, and the remaining "exposed" Oxide layer is removed using an HF vapor process. (see Section 1.2).

However, the HF vapor etch of the Oxide layer also results in a lateral undercut of the Silicon layer. As a result, a length of about 1.8-2.0μm of Oxide is removed from below any exposed Silicon feature edges, including features that are not placed over a TRENCH structure, as shown in Figure 2.4.2.



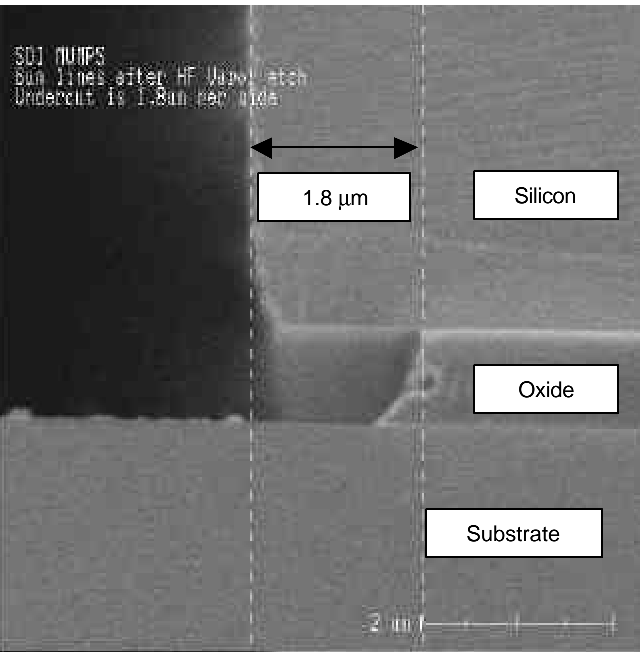


FIGURE 2.4.2 SEM images showing the undercut of the Silicon layer after HF vapor etching of the exposed Oxide layer. The amount of undercut is about 1.8μm per side.

To ensure anchoring of Silicon features to the substrate, the SOI feature size should be greater than 10μm on a side, and should be placed greater than 50μm from the edge of a TRENCH feature (to account for the DRIE etch profile and bias illustrated in Figure 2.3.1). These rules are summarized in Table 2.4.

Desired Effect	SOI to TRENCH Relationship	SOI Feature Size
Release of Silicon Structure	SOI feature enclosed by TRENCH	< TRENCH size
Anchoring of Silicon Structure to Substrate	SOI edge > 50μm from TRENCH edge	> 10μm

TABLE 2.4. Silicon Layer Release and Anchor Rules

2.4.3 Shadow Mask (BLANKETMETAL) Pattern Constraints

The use of shadow masking to provide Metal layer patterning places constraints on the types of METAL patterns that are allowed. The patterns defined by the METAL level produce holes that are etched completely through the shadow mask. As such, no pattern is allowed that would result in "donut" type features being fabricated in the shadow mask, since these features would "fall out" once the etch was completed. Figure 2.4.2 illustrates allowable and unallowable patterns.

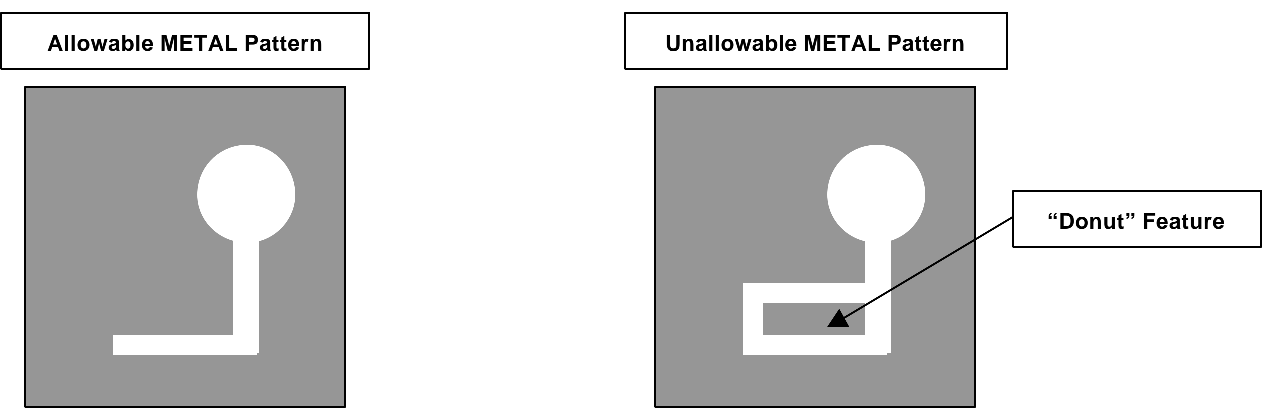


FIGURE 2.4.3. Allowable and unallowable pattern types for the METAL masking level.

2.4.4 Electrical Isolation and Routing

Because there is no insulating layer between the Metal and the Silicon, two adjacent METAL features on the top surface of the Silicon layer will be electrically connected due to the surface doping of the Silicon. As such, patterns in the SOI mask level should be used for electrical isolation between adjacent structures. Undercutting of the Oxide layer during the release etch will prevent Metal step coverage between adjacent SOI features. Figure 2.4.3 illustrates proper and improper patterning of the SOI and METAL levels for electrical isolation. It is acceptable to overlay patterns in the METAL mask level with routing patterns in the SOI mask level to lower the overall resistance of electrical routing paths.

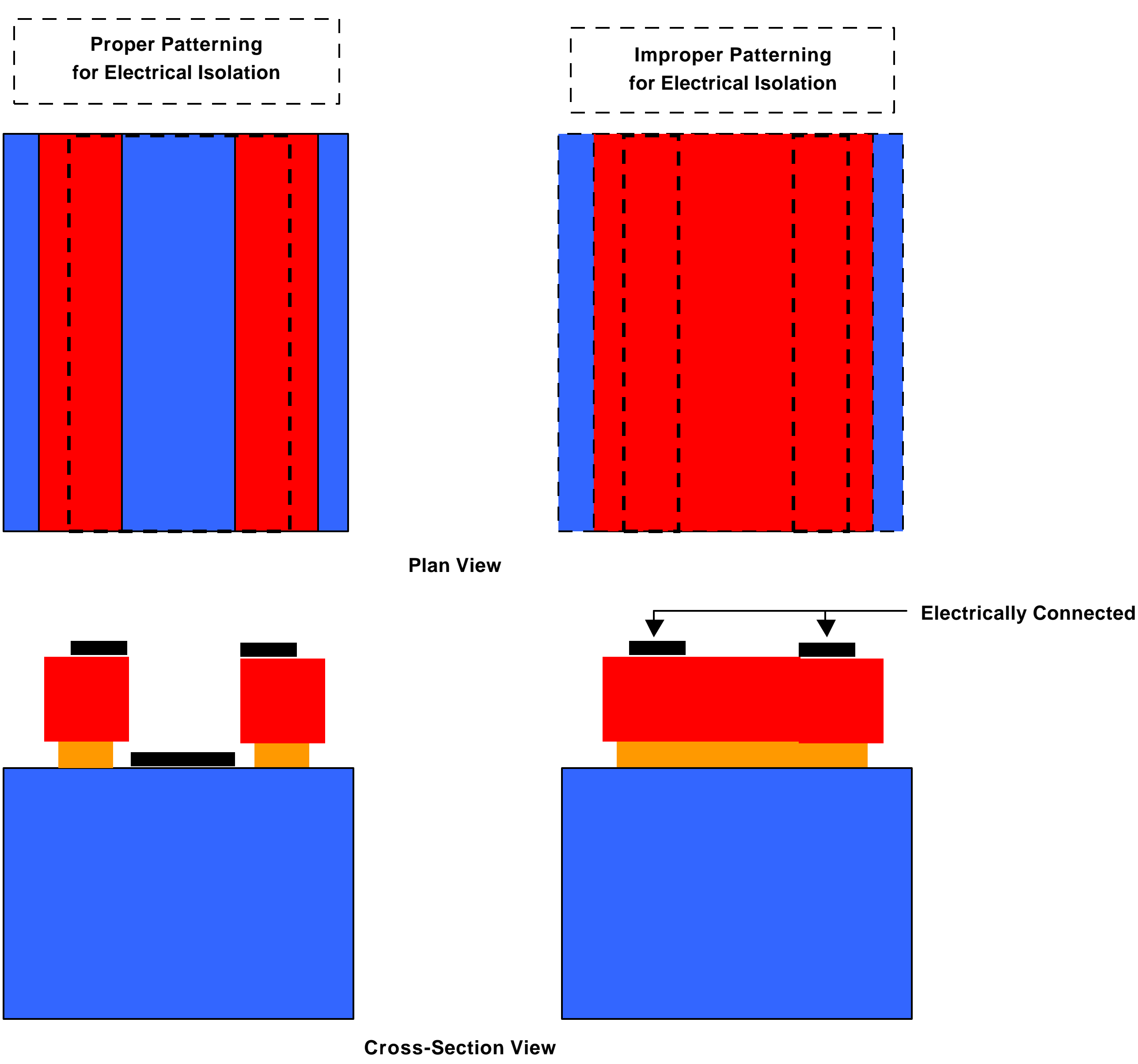


FIGURE 2.4.4. Proper and Improper patterning for electrical isolation

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

2.4.5 Design Features to Avoid Lateral Stiction of Released Silicon Structures

Closely-spaced, long, narrow beams in the Silicon layer may have a tendency to stick together in the release process. For these types of structures, this lateral stiction can often be avoided by incorporating “dimple-like” features into the design. Dimple protrusions reduce the amount of surface area that can come into contact during the release process. (For experienced MUMPs® users, this is analogous to the dimple structures that are used in the polysilicon surface micromachining process to avoid stiction of polysilicon structures to the substrate). Figure 2.4.4 illustrates an example of incorporating dimple features in the SOI mask level to reduce lateral stiction effects in adjacent beams.

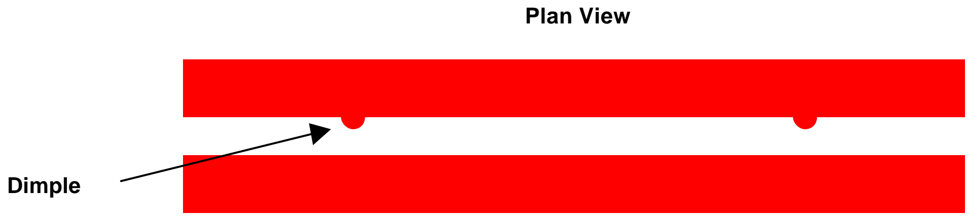


FIGURE 2.4.4. Example of dimple features in the SOI Mask level to reduce lateral stiction affects during release.

2.4.6 TRENCH Pattern Constraints and Full Thickness Suspended Structures

The patterns defined by the TRENCH level produce holes that are etched completely through the Substrate layer. As such, no pattern is allowed that would result in “donut” type features being fabricated in the substrate, since these features would “fall out” once the etch was completed. Figure 2.4.6a illustrates an unallowable pattern in the TRENCH level.

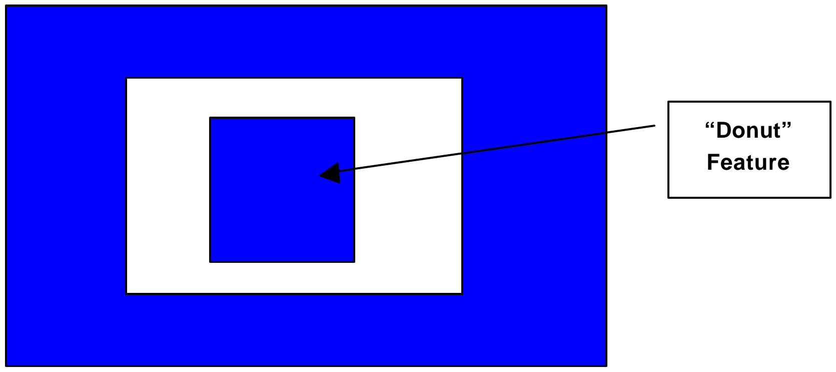
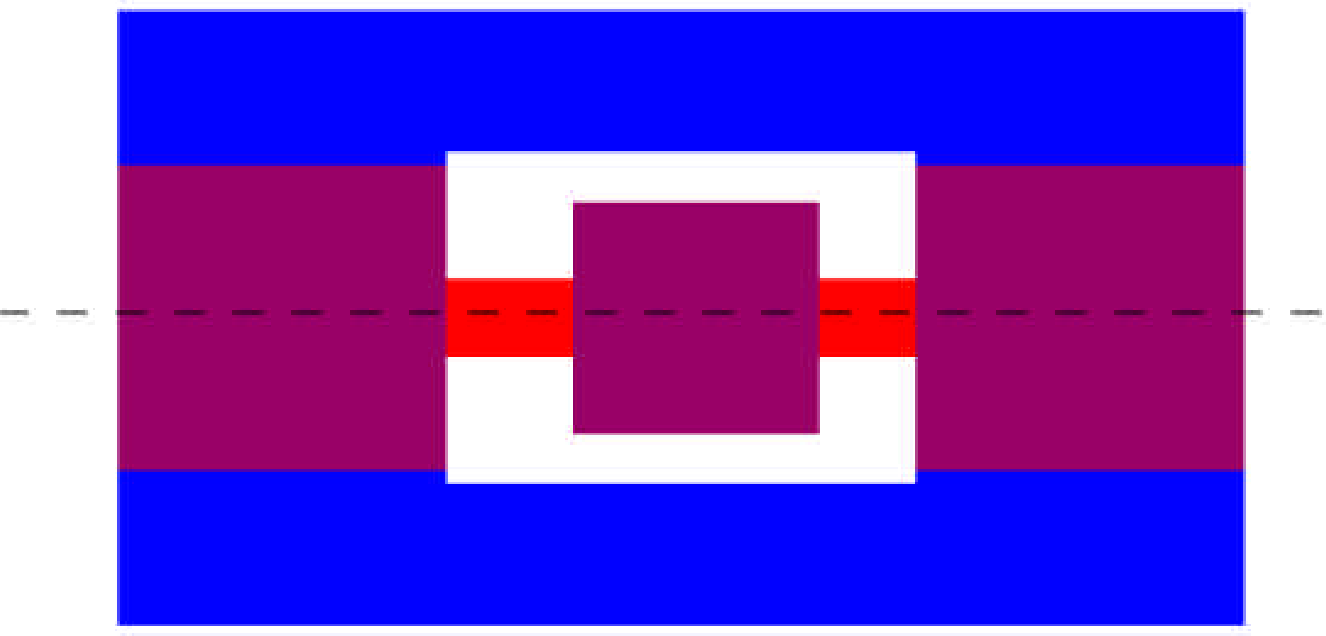


FIGURE 2.4.6A Example of unallowable pattern in TRENCH Level which results in a “donut” feature.

Although it is possible to design a “donut” feature in the TRENCH level that would result in a portion of the Substrate that was supported by the Silicon layer, these “Full Thickness Suspended Structures” typically do not survive the fabrication process. As such, full thickness suspended structures are not allowed in SOIMUMPs. Figure 2.4.6b illustrates a top down and cross sectional view of an unallowable full thickness suspended structure.

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

PLAN VIEW



CROSS-SECTIONAL VIEW

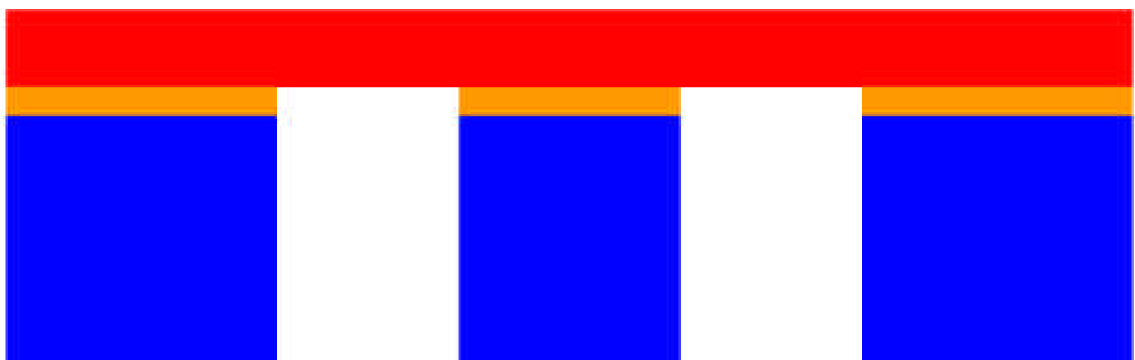


FIGURE 2.4.6B. Example of unallowable "full thickness suspended structure"

	Silicon		Substrate		Bottom Oxide		Shadow Mask
	Oxide		Metal		PSG (dopant)		Frontside Protection Material

2.4.7 Subdicing trenches

By removing silicon in the TRENCH layer and the SOI layer in the same region, the process provides a simple way of subdividing the die into 2 – 4 pieces. The following is a sample layout for this method.

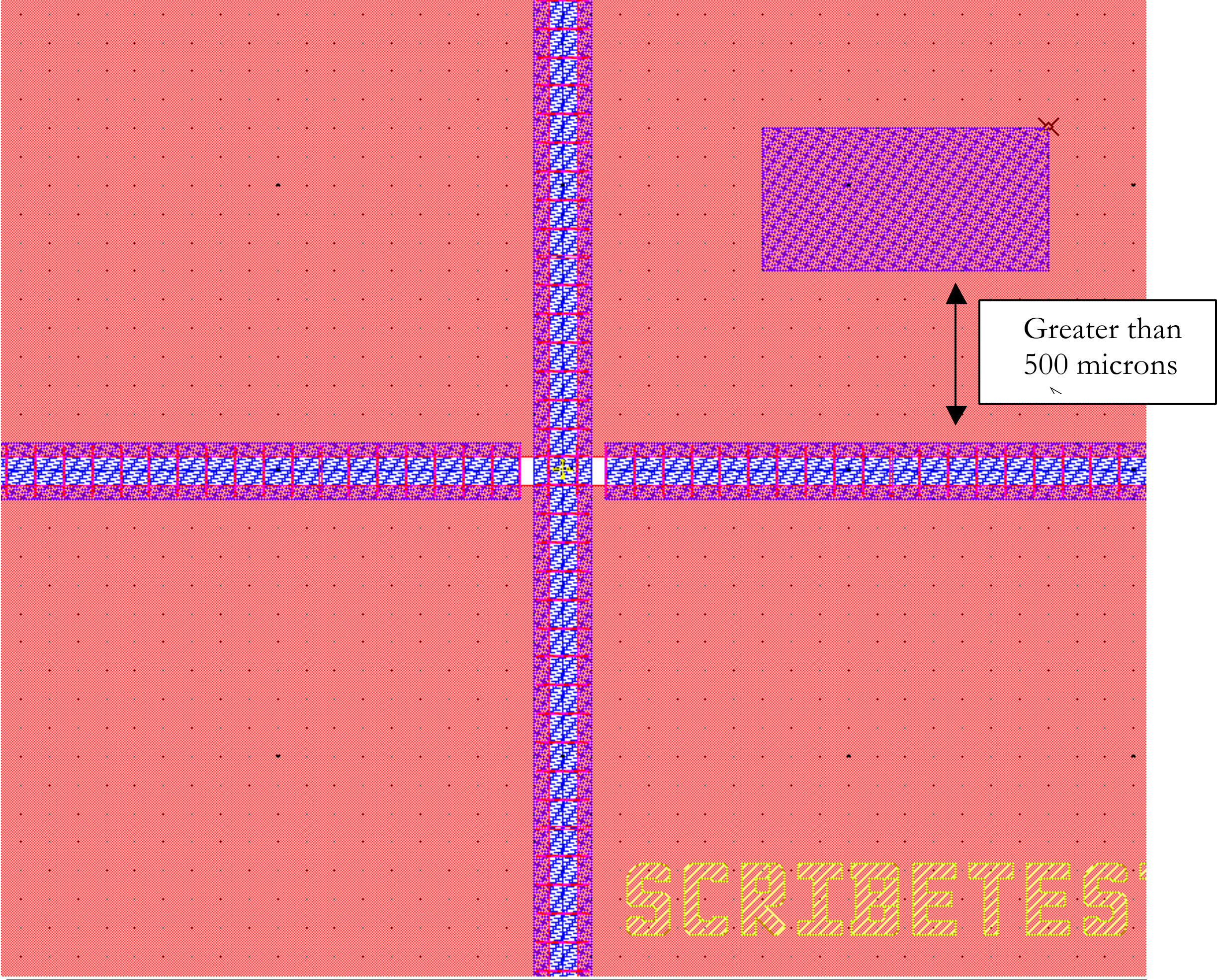


Figure 2.4.7A. SOIMumps Sample intersection used to sub-dice a chip. Trench dimension is 200 micron width running the entire length of the chip; however, it should not intersect. The SOI in each quadrant is tied together with 5 micron strips that are laid out at a 100 micron pitch. Other trench features should not be placed within 500 microns from the streets.

2.4.8 Asymmetric comb drives

Patterns with asymmetric drive combs break much more easily than patterns with symmetric drive combs. This is caused by an unequal expansion force from the protection material deposited on the device layer side of the wafer. Not enough data has been collected to know an appropriate design rule for asymmetric comb drives. Asymmetric comb drive designs with minimum line width structures (2 μm) have shown poor yields.

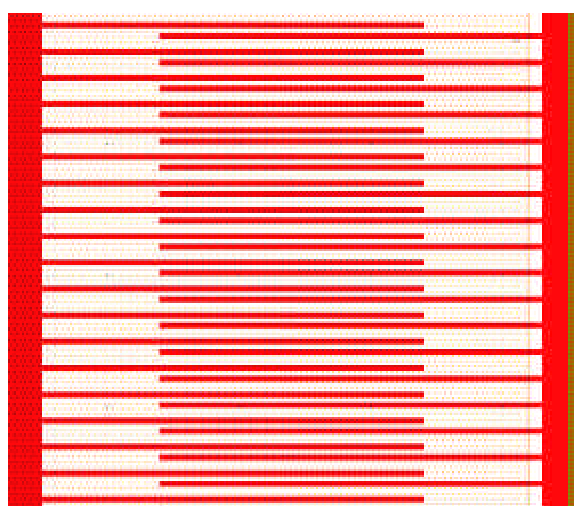


FIGURE 2.4.8A. Sample layout with asymmetric comb finger spacing. The yield using similar finger spacing has been poor. In this case the fingers are 2 microns wide with 2 micron and 4 micron spaces.

2.5 Film Parameters

The thickness and resistivity of relevant layers in the SOIMUMPs process are summarized in Table 2.5. This data is based on measurements from previous runs.

Film	Thickness (μm)			Sheet Resistance (ohm/sq) or Resistivity (ohm-cm)		
	Min.	Typ.	Max.	Min.	Max.	Comments
Pad Metal	0.47	0.52	0.57	0.045	0.065	ohm/sq
Silicon	9	10	11	15	25	ohm/sq (N-type at surface post doping)
				1	10	ohm-cm (N-type in bulk)
Oxide	0.95	1.00	1.05	N/A		
Substrate	395	400	405	1	10	ohm-cm (N-type)
Blanket Metal	0.58	0.65	0.72	.035	.055	ohm/sq

TABLE 2.5. Mechanical and electrical parameters of SOIMUMPs process layers.

2.6 Layout Requirements

2.6.1 Usable Area

The design area for SOIMUMPs is 0.9cm x 0.9cm (9mm x 9mm). Due to the incorporation of an exclusion zone required for the Metal shadow mask bonding process, the actual size of the chips that are shipped to the user is 1cm x 1cm. (The 9mm x 9mm user design area is centered in the chip). Also note that the scribe and break process that is used to singulate the chips produces some particles near the chip edges. Users are advised to place any critical elements of their designs at least 1mm away from the edge of the 9mm x 9mm usable area. (See Figure 2.6.1)

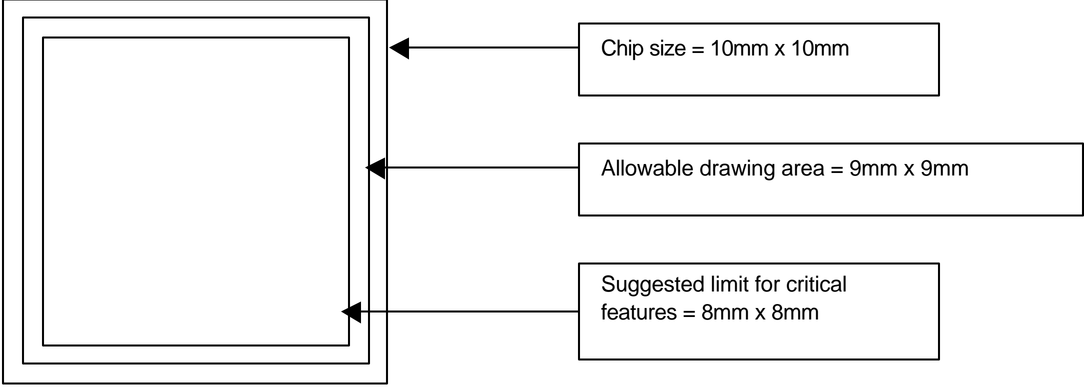


FIGURE 2.6.1: Usable chip area

2.6.2 Cell Name Restrictions

Some errors have occurred in the past due to nonstandard cell names. In order to reduce these errors and the time it takes to translate designs, some guidelines need to be put in place. They are as follows:

1. Cell names should be under 28 characters.
2. Cell names should consist of only the following characters or numerals [a-zA-Z0-9] and the underscore character '_'.

2.6.3 Layer Names

Layouts must use layer names as indicated in Table 2.2. For CIF submissions the indicated names should be used (i.e. for Blanket METAL use BMETL) and for GDS submissions the correct number must be used. Other layers may be in the design; but they will be ignored. MEMSCAP is not responsible for layers omitted due to failure to comply with naming conventions.

2.6.4 General Layout Tips and Known Software Bugs

Mentor Graphics software is currently used to assemble the SOIMUMPs wafers. It does a reasonable job with most translations; however, there are some additional nuances of which users should be aware.

Keep in mind that these are the bugs that MEMSCAP is aware of - we are not responsible for problems resulting from other bugs not listed here.

1. In GDS, three wire types are allowed, extended, butted, and rounded ends. Rounded ended wires will be converted to a truncated ending. *It is strongly suggested that only extended wire types be used with CIF files; otherwise, information may be lost and connections broken.*

2. L-Edit versions 7 and 8, up until version 8.22, have a bug. The bug comes from the donut command in L-Edit which becomes a filled circle when written out to gds and translated into other programs. If you use a donut, be sure to use the horizontal or vertical cut commands to break the donut into multiple polygons.

3. There is a bug in L-Edit versions before 8.41 when working with rotated and mirrored instances. If an instance is rotated and mirrored, then saved to gds, the rotation angle will be rounded off to the nearest degree (i.e. An instance is rotated 22.2 degrees and then mirrored, after saving to gds and reading back in, the angle will be changed to 22 degrees.

   Fix: The cell referencing this instance should be flattened.

4. Mentor will create an error if an illegal polygon is produced during translation. Figure 2.6.4 illustrates an example of this problem. Most layout tools deal with this polygon correctly. To fix the problem the points can be made common or the polygons resized slightly. The user will be responsible for making the changes to fix these errors. These types of errors very often occur in lettering and in pictures that have been translated to gds.

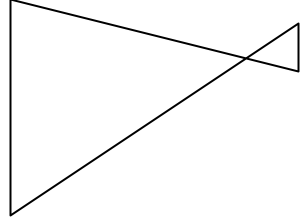


FIGURE 2.6.4A: An Illegal polygon in Mentor.

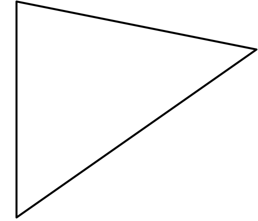


FIGURE 2.6.4B: A Correct polygon.

5. Mentor also has problems with the translations of polygons with numbers of vertices over 1000. These often come from mechanical drawings and should be broken down into smaller polygons before submission.

2.6.5 Design Rule Checking

PLEASE NOTE THAT NO ERROR CHECKING WILL BE DONE ON YOUR DESIGN. We have DRC/technology files available for Tanner, Cadence, and Mentor CAD software. To get these, send an email to *info@memscap.com*.

2.7 Layout Submission

Designs may be submitted in GDSII™ **(preferred)** or CIF formats only. Technology files for L-Edit™, Cadence™, and Mentor's layout tool may be requested via email at *info@memscap.com.*

Before submitting your design, you must complete the Design Submission Form on our website at *http://www.memscap.com/memsrus/svcsres.html*. Once we have received your completed form, you will receive an email with instructions and access information to upload your file to our ftp site.

All designs must be uploaded no later than midnight Eastern Standard Time on the submission due date.