

# Chapter 5

## Soldering Technology for Optoelectronic Packaging

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### 5.1 Introduction

Integration of high speed Internet access, telephone, and cable is a major driving force for fiber-optical network and related technologies. Cost reduction is critical to accelerate the market growth of optoelectronic modules and systems. It is estimated that packaging contributes 60%-90% of overall cost of optoelectronic module (Iezekiel, et. al. 1997), while alignment can contribute up to 90% of the packaging cost. As a result, it is necessary to connect and maintain hundreds of optical precision alignments through a batch assembly process that is compatible with existing manufacturing infrastructure. Soldering is the technology of choice for such a cost-effective assembly process. In addition to providing electrical connections, solder is useful in the formation of passive, precision alignments for optoelectronic packaging. It can be used to couple optical fibers or waveguides to devices such as lasers, light emitting diodes (LEDs), or photodetectors. The alignments can vary from sub- $\mu\text{m}$  to  $\mu\text{m}$  levels for single- or multi-mode fiber applications. Different designs have demonstrated precision alignments, and the aligned structures are becoming more and more complex (Lee and Basavanhally, 1994).

Solder has been used widely as a die-attach material for optoelectronic packaging, and its application range is being further expanded because of the development of the flip-chip assembly. Flip-chip soldering was introduced by IBM as the controlled-collapse chip connection (C4) soldering technology (Miller, 1969). Since then, many advantages of the technology have been realized: superior electrical performance, high reliability, reduced footprint, high I/O density, low cost, efficient heat conduction, batch assembly and self-alignment during the chip jointing. In particular, batch assembly capability and the self-alignment mechanism are critical to precision optical alignments.

Figure 1 illustrates the mechanism of solder self-alignment. As the temperature of the solder is raised above its melting point, the molten solder starts wetting the metal pad and moving the chip. The chip movement is driven by a surface tension force in an effort to minimize the surface area to reaching the lowest total energy of the assembly. At the final position, the system will have the lowest total energy, and the position of the chip is locked by cooling the solder joint. Using solder,

hundreds or thousands of such alignments can be accomplished with a single batch reflow process, and the cost/alignment can be reduced by orders of magnitude.

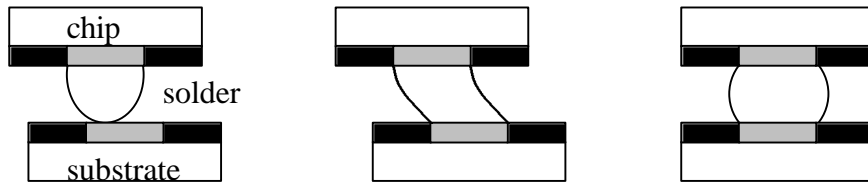


Figure1: Self-alignment of soldering technology

Different soldering technologies have already been developed for various optoelectronic modules. The packaging strategies have been focused on precision alignment. This chapter will present representatives of the modules in different categories defined by the roles of the solder. For a detailed understanding of the technology, we will review a case study of NEC's Au/Sn-based optoelectronic assembly technology. In addition, critical issues will be discussed with an emphasis on solder materials, fluxless reflow, design and reliability.

## 5.2 Solder Assembled Optoelectronic Modules

Table 1 lists 18 cases taken from 68 solder-assembled modules reported between 1990-1997. The number of publications in this area has increased significantly recently; therefore, the review could not cover all the publications. The 18 studies are listed in the reference section; other publications reviewed were listed in Tan and Lee (1996). Solder has been used to align photonic device to substrate or chip carrier or fiber, fiber to photonic device, and microlens to photonic device. Their alignment methods varied from active to passive ones with or without solder self-alignment, and the alignment accuracy ranged from  $\pm 5$  to  $0.5 \mu\text{m}$ . The metallization used Ti or Cr as the adhesion layer, Cu, Ni, or Pt as the barrier metal and Au coating to prevent surface oxidation. Length scales (diameter or width) of the solder bumps varied from 26 to  $330 \mu\text{m}$  and heights ranged from 5 to  $50 \mu\text{m}$ . The solder materials were eutectic 63Sn/37Pb, In, 50In/50Pb, or eutectic 80Au/20Sn. The solder reflow used liquid flux, formic acid vapor, or forming gas. Couplings were efficient for single- or multi-mode applications.

Representatives of the modules will be further reviewed with the following four assembly categories: 1) solder assembly with no precision self-alignments, 2) self-aligned solder assembly with no mechanical stops, 3) self-aligned solder assembly with one mechanical stop, and 4) self-aligned solder assembly with two mechanical stops.

### 5.2.1 Solder assembly with no precision self-alignments

In this assembly category, solder is used to provide electrical connections and maintain mechanical connections for optical alignments. Solder self-alignment is not an important concern. Figure 2 shows an optical head for CD-ROM drives (Nagano et al., 1993). The photodetector was used as a substrate to carry a preamplifier through flip-chip soldering and a laser diode through die-bonding. Before the bonding, the laser diode's position was adjusted according to an alignment mark on the photodetector. With the preamplifier and the laser diode, the photodetector assembly was flip-chip soldered to a ceramic case to form a very compact module. This solder assembly approach was better than wire bonding approach because of its reduced size, electromagnetic noise, capacitance and inductance. In addition, the design increased the alignment tolerance between the optical module and a hologram element since the distance between the photodetector assembly and a glass window was well controlled. The module was 6mm×6mm×1.64mm and 0.25 g, which was much smaller and lighter than the old module (7.5mm×8mm×3.05mm and 0.6g).

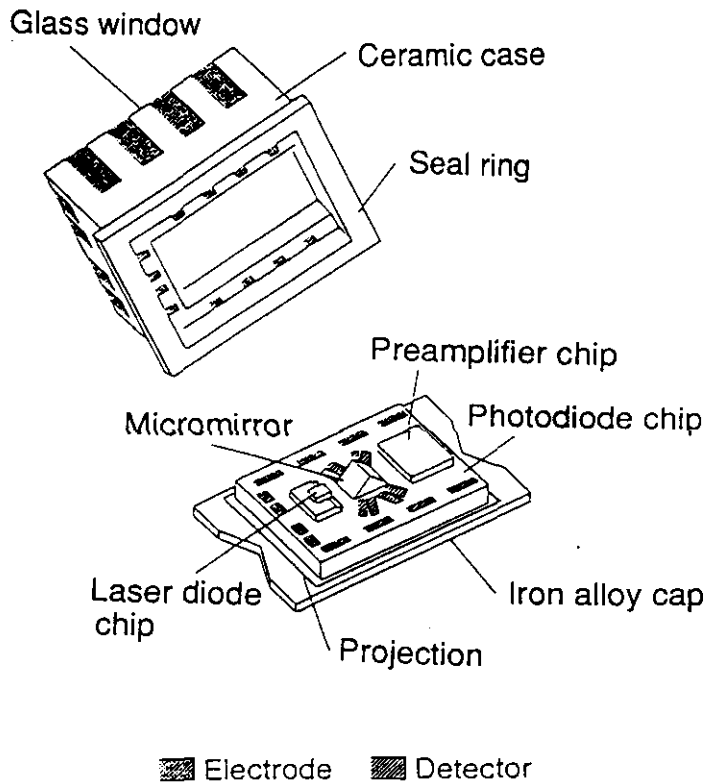


Figure 2: Optical head for a CD-ROM drive.

Table. 1 Examples of optoelectronic modules using solder

Package	Alignment method and Accuracy ( $\mu\text{m}$ )	Solder bumping and size ( $\mu\text{m}$ )	Solder material	Metallization	Reflow Atmosphere / Temp.	Main Feature	Reference
LD on Silicon Mother-board	$\pm 20$ and $5^\circ$ tilt →self-aligned	Height: 8.5	Pb/Sn Eutectic	Cr/Cu/Au	flux	Hybrid assembly	GEC-Marconi Edge, 1991
LED/PD on AlN submount	Self-aligned 3	electrical plating 150×400×50	Pb/Sn	Cr/Ni 0.1 $\mu\text{m}$ /0.2 $\mu\text{m}$	180°C		NEC Itoh, 1991
Si chip on glass	Self-aligned 0.8	Evaporate Dia: 130 $\mu\text{m}$	50%In/ 50%Pb	Ti/Cu/Au		Long term alignment stability	NTT Hayashi, 1992
High speed photo-receiver	Self-aligned 0.5	Lift-off photoresistor Dia: 25	Pb/Sn or In			Micro-solder bump	NTT Tsunetsugu, 1992,1996
LED print head	self-aligned					self-align a row of LED	HP Haitz, 1992
Laser on Wafer board	Mechanical stop $\pm 1$		In	Ti/Ni/Au	flux 200°C	mech. stop only	GTE Armiento, 1992
LD on Si substrate	Self-aligned $\pm 3 \rightarrow \pm 1$	Mechanically formed Dia: 50	80Au/ 20Sn eutectic			Au/Sn solder alignment	NEC Sasaki, 1992
Optical fiber alignment	self-alignment for fiber					fiber $\perp$ substrate	IBM Blacha, 1993
Photo-detector on Si	Self-aligned $\pm 60 \rightarrow \pm 2$	E-beam evaporation Height: 5	Au/Sn Eutectic	Ti/Pt/Au	gaseous formic acid	Fluxless	AT&T Deshmukh, 1993
VLSI/FLC SLM	Self-aligned $\pm 2$ Self-pulling gap uniformity:0.3	Dia: 105	63Sn/ 37Pb		forming gas	Mixed joint design	U. Colorado Lin, 1993 Ju, 1993
Optical head for CD-ROM	Mechanical aligned					Flip-chip used for save space	NEC Nagano, 1993
OEIC transceiver	Self-aligned X: $\pm 2$ Y: $\pm 0.75$ vertical standoff	Dia: 125 $\mu\text{m}$	Pb/Sn	Ti/Ni/Au Cr/Cu/Au	flux	self-alignment and mech. Stop	IBM Jackson, 1994
Optical subscriber system	Self-aligned $\pm 3$ standoff	thermal evaporate Dia: 50			flux	self-aligned/ standoff	ETRI Lee, 1995
LED on Silicon	Self-aligned $\pm 5$	330×330×25	Au78/ Sn22	Ti/Pt/Au	formic acid 300-320°C		AT&T Dautartas 1995
Multiplex data link	Active aligned		Au/Sn	Au/AuZn		Solder for fiber fixing	Fujitsu Yano, 1995
LASER-PAC	$\pm 50 \rightarrow$ Self-aligned	Evaporated thickness 6	Au80/ Sn20	Ti/Pt/Au	fluxless	Batch aseembly	Bell Labs, Gate, 1996
free space module	Self-aligned $< 2$	Electroplated Height 30	Eutectic Pb/Sn	Cr/Cu/Au	flux	Align microlen to VCSEL	U. Maryland, Pusarla, 1996
Waveguide module	Lateral alignment $< 2$		Pb/Sn	Ti/Cu	Formic acid	Controlled self-alignment	U. Colorado Morozova, 1997

Figure 3 shows another solder application for optoelectronic packaging. A hybrid transmitter module was developed by using the Silicon Waferboard Technology and solder (Armiento et al., 1992). As shown in the figure, pedestals and standoffs were used to define the chip position during robotic placement. They were precisely micromachined thus permit the placement of the laser array to an accuracy of  $\pm 1\mu\text{m}$ . The height of the standoff was larger than that of the deposited solder thickness. A gram-level force was applied to the laser array during the solder reflow process. The solder raised to wet the solder pad on the laser, and the laser was held in contact with the standoffs and pedestals. The assembly accomplished precision alignments with coupling efficiencies comparable to those achieved with active alignments. Solder joints were used to provide electrical contacts and maintain the alignments.

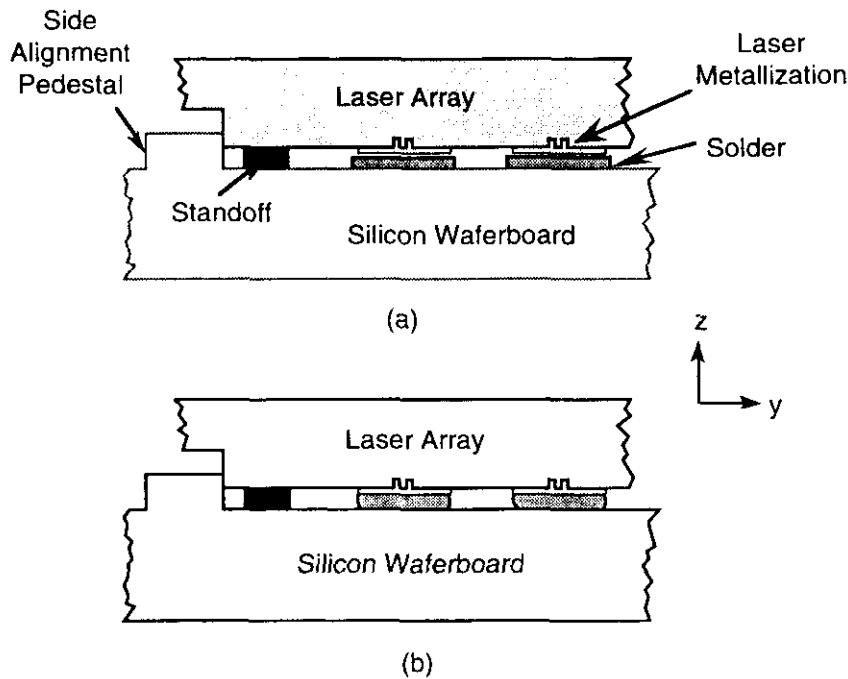


Figure 3: Precision assembly using standoffs, pedestals, and solder: a) before reflow, b) after reflow.

### 5.2.2 Self-aligned solder assembly with no mechanical stops

As shown in Figure 1, solder self-alignment can align a component to a substrate automatically during a reflow process. Such a mechanism was used by Deshmukh et al. (1993) and Nordin et al. (1992), which were reviewed by Lee and Basavahally (1995). Figure 4 illustrates another case demonstrated by Hayashi et al (1992). The module was similar to a conventional pig-tail module. It aimed at providing a package solution for photo-diode(PD), light emitting diode (LED), and vertical-cavity surface-emitting laser (VCSEL). A zirconia ferrule was integrated with an alumina chip carrier as the

packaging platform. The photonic device was self-aligned to the chip carrier using solder. Experiments were carried out to achieve the optimum alignment result. These experimental works showed that alignment accuracy improved as the bump diameter decreased and/or number of bump increased. Submicron ( $0.5\mu\text{m}$ ) alignment accuracy was achieved by using 32 micro-solder bump with a diameter of  $25\mu\text{m}$ .

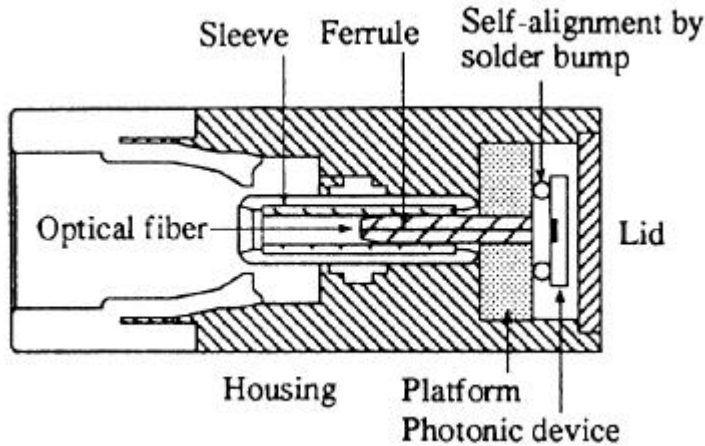


Figure 4: Optical module using platform with optical ferrule.

Figure 5 is another self-aligned design disclosed in US patent 5247597 by Blacha et al., (1993). An alignment chip was bonded to the silicon substrate. There was a via hole in the alignment chip which defined the fiber position. The coupling loss was less than 1dB for one of the modules measured. A similar approach for an optical link perpendicular to a substrate was also reported by Benzoni and Dautartas (1994) and Dautartas et al. (1995). These self-aligned designs are ideal for the alignment between fibers and surface emitting or receiving devices, which are important to high-density integrated optoelectronic modules.

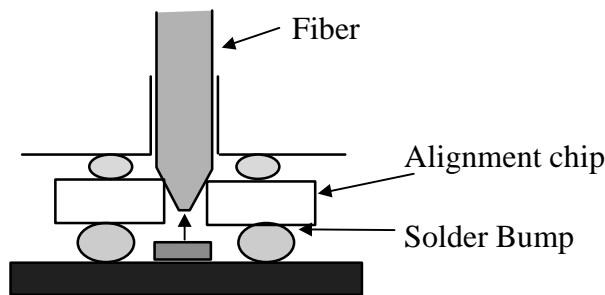


Figure 5: Optical fiber in an alignment chip soldered onto a substrate.

Figure 6 shows a free space optical connect module developed by Pusarla, et. al. (1996). Self-aligning soldering was used to align Photoresist Refractive Optics by Melting techniques (PROM) microlens array and PD array. The fabrication process is described as follow. The PD chip was first bonded to a silicon substrate. Photoresist was then spin coated on the PD and then soft baked, exposed and developed to define the pattern of solder wettable pads. Cr(300A) /Cu(3000A) /Au(300A) was then thermally evaporated and the photoresist was lifted off. Microlens array was fabricated on the top side of the glass substrate using AZ4903 photoresist. Then Eutectic Pb/Sn solder was deposited on the bottom side of the glass substrate. Agian, Cr/Cu/Au was thermally evaporated first. Then AZ4904 photoresist was spin coated, softbaked, and eposed. A 30µm solder layer was then electroplated and the photoresist was washed away using acetone. The microlens module was then fluxed, reflowed, fluxed and bonded to the PD chip. The self-alignment accuracy was less than 2µm.

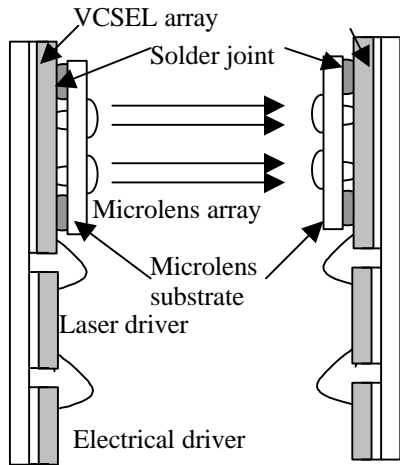


Figure 6 Free space VCSEL-to-microlens-to-Photodiode optical connect structure

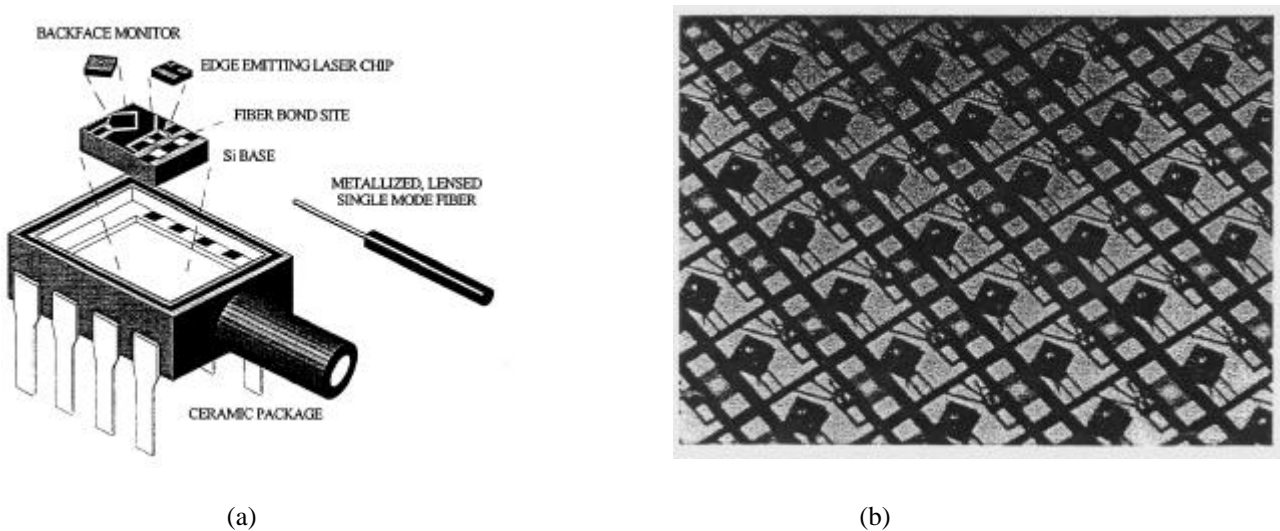


Figure 7 LASER-PAC module a) LASER-PAC b) wafer level assembly

The self-aligning feature of soldering makes it very suitable for batch assembly. Figure 7 shows an edge emitting laser module developed by Gates, et. al.(1996). The Optical Sub-Assembly (OSA) for this package was assembled at wafer level using solder. The OSA contained a silicon substrate, a backface monitor chip and an laser chip. It also had a site for fiber bonding. Ti/Pt/Au (1kA/2kA/5kA) were sputtered, and 6 $\mu$ m of Au/Sn (80/20) was evaporated on the laser and detector chips. The chips were first attached to the wafer using thermocompression bonding at a pick-and-place accuracy of  $\pm 50\mu$ m. Then the assemblies were reflowed at wafer level in a controlled atmosphere. Solder bumps were used only to self-align the chip. Electrical connections were provided by wire bonding. These OSAs could be electrically probed and inked to identify poor devices. After testing, the Si wafer was diced for OSA separation. More than 2000 OSA can be assembled at one reflow step.

### 5.2.3 Self-aligned solder assembly with one mechanical stop

The solder self-alignment force can be separated into two components: one is the restoring force that moves the component laterally and the other is the pulling or pushing force that moves the component vertically. Unfortunately, these two force components are proportional to the misalignment and become very small when the component is close to the well-aligned position. If a strong force is desirable for precision alignments, it is preferred to use misaligned solder joints and mechanical stops. Figure 8 shows a mechanical stop to controlling the lateral motion for a vertical alignment or a standoff for the gap (height) control. The misaligned molten solder could push the stops against each other to achieve the precision alignments. Since the force is proportional to the misalignment or spacer height, it can be orders of magnitude larger than that with respect to a nearly well-aligned solder joint.

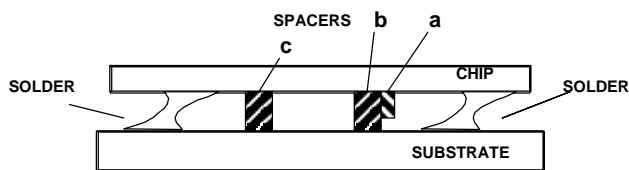


Figure 8: Self-aligned solder assembly with one mechanical stop using spacers a and b for the horizontal stop or b and c for the vertical standoff.

Figure 9 is an optical subscriber interface system developed by Lee et al. (1995). The laser submodule had two V-grooves in a row, one was for the single-mode fiber, and the other was for guiding light from the rear mirror plane of the laser to a monitor photodetector. Both laser diode and photodetector were flip-chip soldered to a silicon substrate. In addition to using

solder self-alignment for the lateral alignment, a Au standoff was used to control the height of the laser. The lateral alignment accuracy reached  $\pm 2\mu\text{m}$  and the height control was within  $\pm 0.7\mu\text{m}$ .

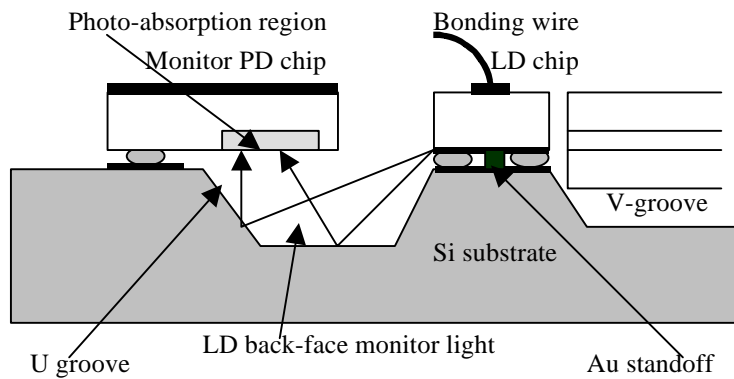


Figure 9: Silicon mounts for an optical transmitter module using a standoff.

Figure 10 shows another case using solder self-alignment and a mechanical spacer for a spatial light modulator (Lin et al., 1993 and Ju et al., 1993a). During reflow, the large solder joints pulled the cover glass with mechanical spacers toward the VLSI; these two components formed a uniform gap to be filled with ferroelectric liquid crystal. The compliant surface tension force assured a good gap control, and the soldering process was compatible with the existing solder-based manufacturing infrastructure. A  $\mu\text{m}$ -level gap with a sub- $\mu\text{m}$ -level uniformity was accomplished.

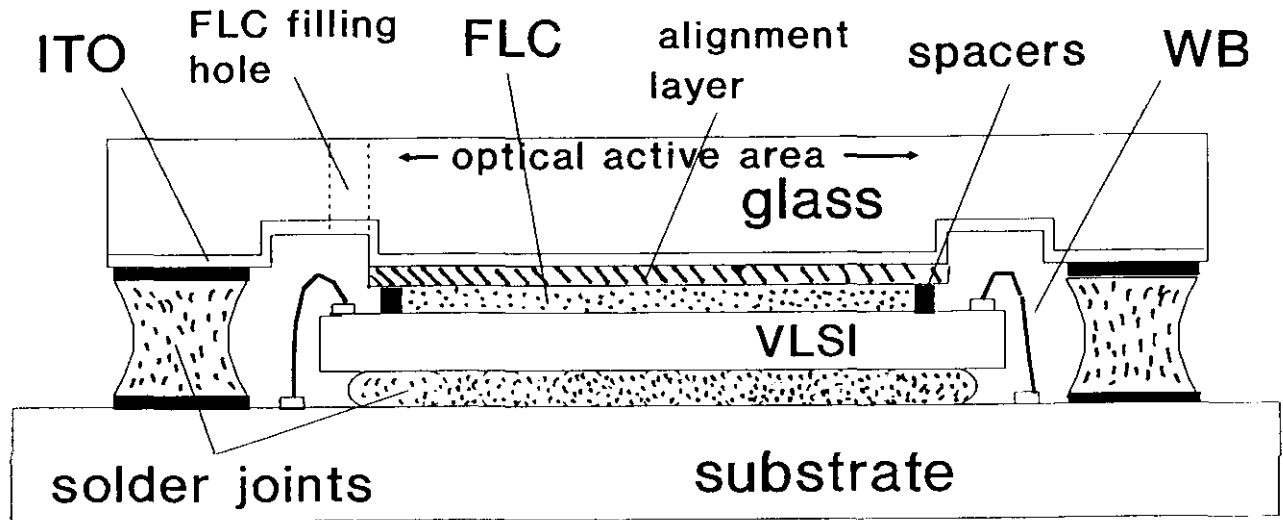


Figure 10: Solder-assembled liquid crystal-on-VLSI.

#### 5.2.4 Self-aligned solder assembly with two mechanical stops

The lateral and the vertical mechanical stops shown in Figure 8 can be integrated using all three spacers a, b, and c in a single module design. Figure 11 is a photo of such a module developed by Jackson et al. (1994) for a four-channel transceiver. The mechanical stops were used to define the position and the height of the laser array that was connected to the planar waveguide for routing optical signals. The use of mechanical stops reduced the effect of solder volume variations on the alignment accuracy. The final misalignment reported was  $\pm 2.0\mu\text{m}$  for the lateral and  $\pm 0.75\mu\text{m}$  for the height control. The coupling loss was between 3.9 and 4.2dB.

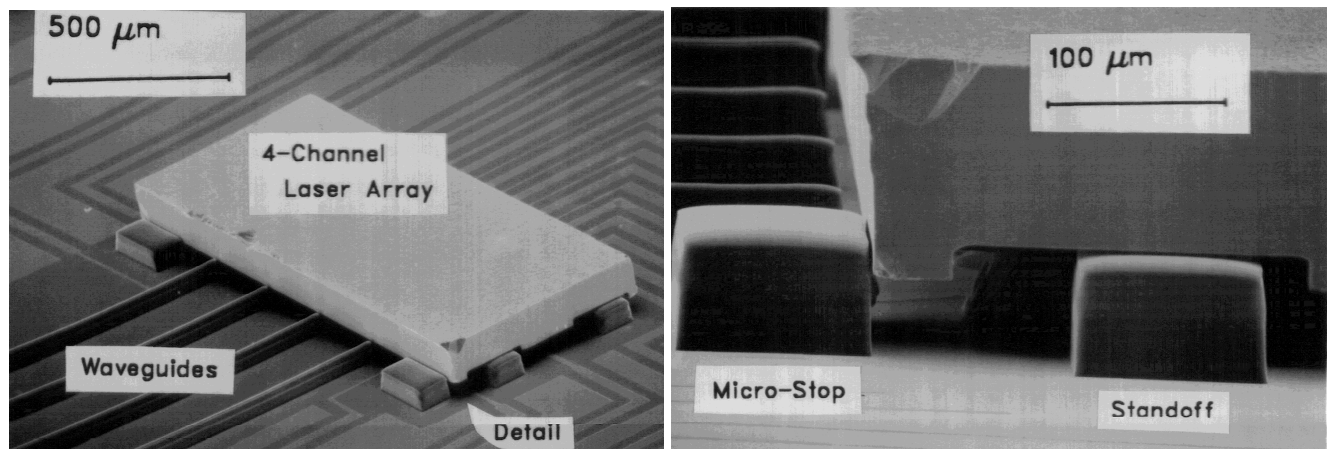


Figure 11: Four-channel laser array using two mechanical stops and misaligned solder joints.

### 5.3 Case Study: AuSn Solder Flip-chip Bonding and Its Module Applications

In addition to the above overview, we will present a case study to discuss some packaging details. In particular, a Au/Sn soldering technology and its applications will be presented. To maintain reliable precision solder alignments, hard solder such as AuSn is required to avoid solder creep (Sasaki, et. al. 1992). This case study shows a three-dimensional passive alignment technology of optoelectronic devices using AuSn solder bump flip-chip bonding. The study will address three issues: bumping technique, stripe-type bump bonding and applications.

#### 5.3.1 Bumping Technique

In solder bump flip-chip bonding, soft solder such as Pb/Sn or Pb/In is used for bump material because it makes bump fabrication easy. However, a LD/PD chip mounted with such soft material tends to move out of alignment due to solder creep as time passes, and this may cause additional coupling loss. Furthermore, the use of flux in the optical chip mounting reduces chip reliability. To solve these problems, hard solder such as AuSn should be used. However, fabricating AuSn solder bumps poses a specific difficulty. Conventional electroplating technique is not feasible because of the difficulty of precisely controlling both the ratio of Au/Sn and solder volume. Similarly, vacuum deposition is impractical because of the high cost incurred due to the many unavoidable processes involved in vacuum deposition of films with thickness of tens of micrometers.

To solve this problem, an AuSn solder bump fabrication technology has been developed in which Au-Sn bumps are mechanically fabricated using a combination of micro punch and die (Itoh, et. al. 1996a, 1996b), as shown in Figure 12. Firstly, a AuSn alloy ribbon was punched into a small piece with a micro punch and a die onto the submount. The submount was heated and placed under the punch and the die. It was then positioned so that the electrode on which the piece to be provided was just under the punch.

The submount and the punch were moved synchronously with the punching operation. The punched piece was provided by the surplus force of the punching operation onto the electrode pad of the submount in a successive manner. Since the submount was heated in advance, the bonding metal piece of AuSn alloy was alloyed with the Au film of the electrode pad to form an alloy layer by the thermocompression bonding, so that the piece could be bonded to the electrode pad. After all the pieces were produced, the submount was heated to the melting point of 280°C to form the solder bumps.

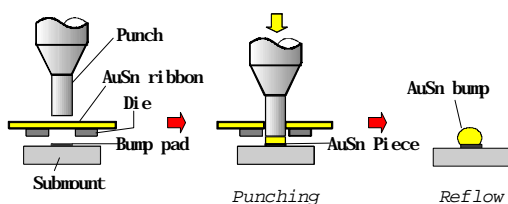


Figure 12 AuSn bump mechanical fabrication technique

Figures 13(a) and (b) are SEM photographs of punched AuSn pieces and AuSn solder bumps after reflow, respectively.

Figure 14 is a histogram of solder bump height for the case with the punch diameter of 90 $\mu\text{m}$  and the die diameter of 100 $\mu\text{m}$ .

The AuSn ribbon was 80%Au-20%Sn eutectic solder and its thickness was 30 $\mu\text{m}$ . Bumps with a height accuracy of  $\mu\text{m}$  were successfully fabricated. A high aspect ratio between the bump height and the pad diameter was required for the bumps to

achieve a surface tension level needed for a good self-alignment in the horizontal direction. Figure 15 is a histogram of the accuracy of the horizontal self-alignment of the optical array chips in the case with 50  $\mu\text{m}$  bump diameter and 50  $\mu\text{m}$  height.

An accuracy of about 1 $\mu\text{m}$  was obtained. The new bumping technique enabled an engineer to form the AuSn solder bumps easily and accurately even when a submount could not accommodate electroplating or vacuum deposition. The technique it is extremely high in productivity and low in cost.

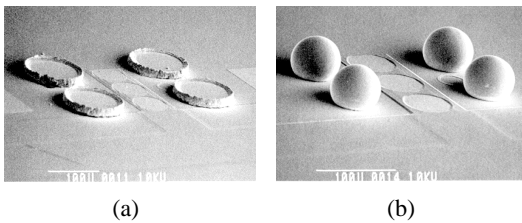


Figure 13(a)Punched AuSn pieces, (b)AuSn bumps after reflow.

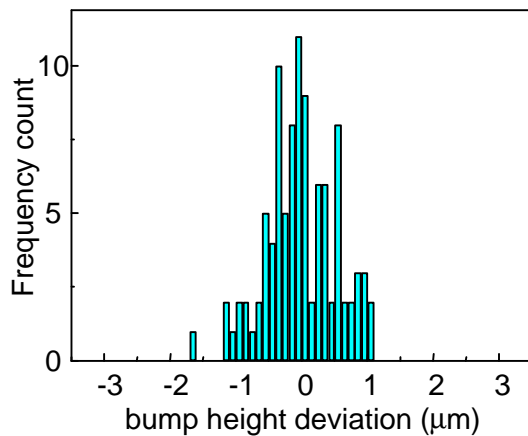


Figure 14 Bump height deviation

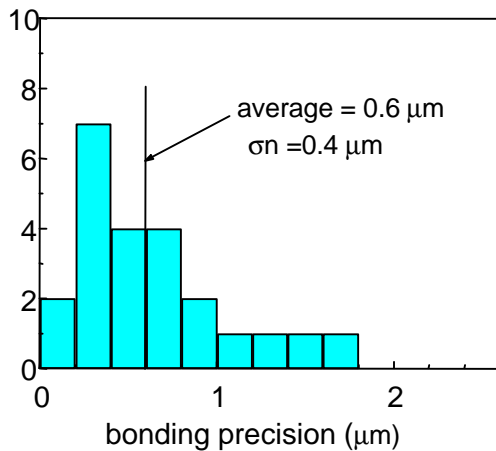


Figure 15 Horizontal self-alignment accuracy of optical chips.

### 5.3.2 Stripe-Type Bump Bonding

In the case of laser diode-single mode fiber (LD-SMF) coupling, very accurate three-dimensional chip alignment (within  $1\mu\text{m}$ ) is required. In spherical bump bonding, bonding height deviation, which is mainly affected by the unavoidable solder volume deviation, is  $1.5 - 2.0\mu\text{m}$  for the  $50\mu\text{m}$  bump diameter usually used for LD chip mounting. Lowering spherical bump height itself may reduce the bump height deviation. However, it results in a decrease in the aspect ratio, which then decreases the surface tension to a level below that required for the effective self-alignment. Reducing the spherical bump diameter may also reduce the height deviation. However, many smaller bumps are required to achieve the surface tension sufficient to move the LD chip, and this increases bump fabrication cost. Furthermore, reducing the bump size creates a need for precision placement of LD before the reflow process.

An alternative stripe-type bump flip-chip bonding technique has been developed (Itoh, et. al. 1996b, Sasaki, et. al. 1995) in order to improve the bonding height precision. Figure 16 shows SEM photographs of the punched AuSn pieces and of the stripe-type AuSn solder after reflow. Figure 17 shows the self-alignment achieved by these stripe-type solder bumps. The left photograph is before reflow, and the right one is after reflow. The precise self-alignment due to the stripe-type AuSn solder bumps is clearly demonstrated. In this technique, the ratio of bump height/stripe width is important to good self-alignment in the horizontal direction. The ratio plays a role different from the aspect ratio for the spherical bump bonding. Spherical solder bump height could not be reduced without reducing solder volume under a fixed aspect ratio. On the other hand, with stripe-type bumps, bump height could be reduced while both solder volume and aspect ratio remain unchanged. The bump width and length could be selected individually. Figure 18 shows histograms of bonding height precision for stripe-type bumps (upper) and spherical bumps (lower). In the stripe-type bump bonding, the stripe width was  $20\mu\text{m}$ , the length was  $140\mu\text{m}$ , and the bonding height was  $20\mu\text{m}$ . In the spherical bump bonding, the bump diameter was  $50\mu\text{m}$  and the bonding height was  $40\mu\text{m}$ . This result shows that the use of stripe-type bumps significantly improved vertical precision. Figure 19 is a histogram of horizontal alignment accuracy of the optical array chips. High accuracy of less than  $1\mu\text{m}$  is obtained.

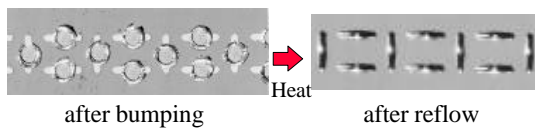


Figure 16 Stripe-type AuSn bumps.

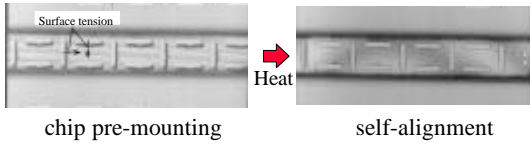
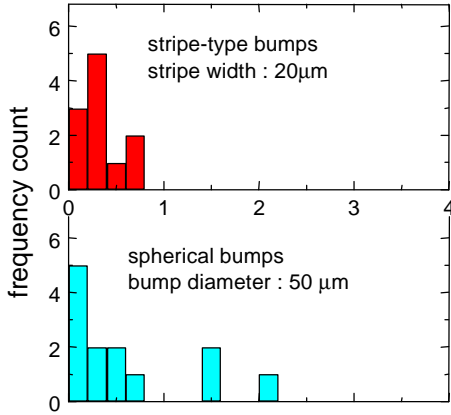


Figure 17 Self-alignment effect for stripe-type AuSn bumps.



bonding precision in vertical direction (µm)  
Figure 18 Bonding height precision for stripe-type AuSn bumps.

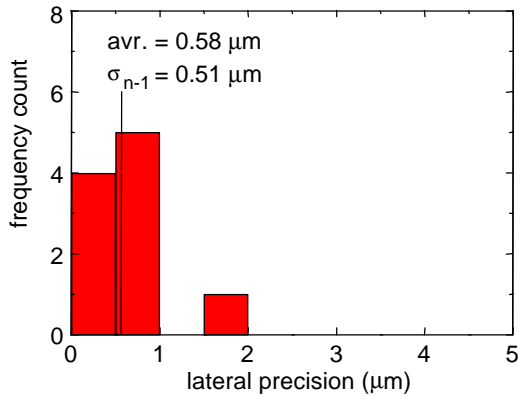


Figure 19 Horizontal bonding precision for stripe-type AuSn bumps.

### 5.3.3 Applications for Optical Module Si Benches

A. PD Array Module: Figure 20 shows the schematic diagram of a PD array module optical platform. The output light beams from the optical fiber array are reflected upwards from metallized Si V-groove ends and coupled to the PD array's light receiving regions. The PD array chip was mounted on the Si substrate by AuSn solder bumps. Spherical solder bumps were used since PD chip alignment tolerance was more than 5µm. The micro punch and die technique was applied to deposit AuSn solder alloy pieces onto ten solder pads of 70µm diameter on the submount. The diameters of the punch and the die were 90µm and 100µm, respectively. The AuSn alloy ribbon was 80% Au-20% Sn eutectic solder with a thickness of 40µm. The submount was heated to melt the AuSn solder, which balled up to a height of 70µm. The PD array was a monolithically integrated 1x8

linear array, employing InGaAs/InP PIN PDs, each with a 80 $\mu\text{m}$  light receiving diameter, spaced at a 250 $\mu\text{m}$  pitch. The PD array chip was placed face-down on the spherical AuSn bumps, and the submount was heated in N<sub>2</sub> atmosphere to melt the solder. No flux was used. The surface tension of the molten solder aligned the PD array chip automatically (see Fig.21) (Itoh, et. al. 1996a). Three-dimensional alignment accuracy was within  $\pm 2\mu\text{m}$ . Figure 22 shows the PD array module optical platform, composed of the PD array and the fiber array. The fiber array contained 8 graded-index, multimode fibers (MMFs) spaced at a 250 $\mu\text{m}$  pitch. Each fiber had a core diameter of 62.5 $\mu\text{m}$  and was tipped with a microlens produced by chemical etching (Honmou, et. al. 1996) to reduce the coupling loss to the PD array. The lens radius was set to approximately 50 $\mu\text{m}$  in order to keep the optical output light spot size to be within 80 $\mu\text{m}$  of the PD light receiving diameter. The fiber array was placed into the V-grooves on the Si submount. These V-grooves had been made by an anisotropically wet etching process and had dimensions controlled to within  $\pm 1\mu\text{m}$ .

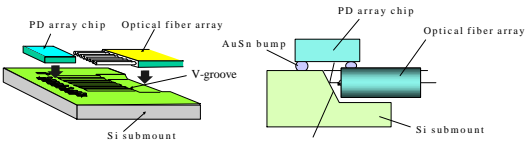


Figure 20 PD array module optical platform schematic diagram.

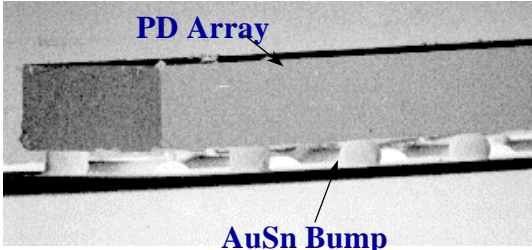


Figure 21 PD array chip bonded AuSn solder bumps.

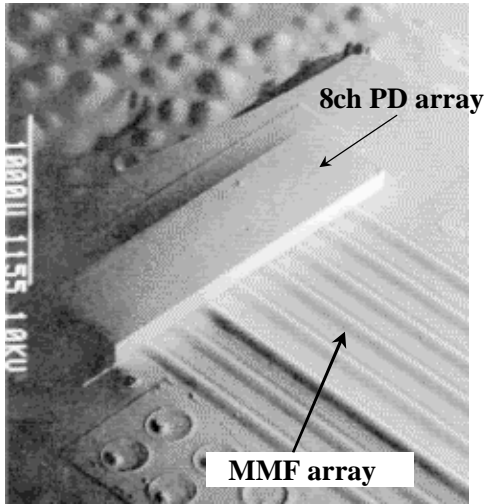


Figure 22 PD array module optical platform.

**B. LD Array Module:** The LD output light beams are coupled directly to a flat end 8-channel optical fiber array. A slit was fabricated on the Si submount by a dicing saw so that the fiber end could be brought close to the LD facet. The fiber was embedded in the Si V-grooves in the same manner as in the PD submount. Figure 23 shows the LD array module optical platform (Itoh, et. al. 1997), composed of the LD array and the flat end fiber array. The LD array was a monolithically integrated 1x8 linear array, employing 1.3 $\mu\text{m}$  wavelength InP/InGaAlP LDs with a 250 $\mu\text{m}$  pitch. The LD array chip was bonded on the stripe-type AuSn bumps in the same manner as in the PD chip bonding without flux in N<sub>2</sub> atmosphere. Figure 24 shows the stripe-type bumps on the Si optical bench before LD chip bonding. The fiber array contained 8 single-mode fibers spaced at a 250 $\mu\text{m}$  pitch. Each fiber had a core diameter of 10  $\mu\text{m}$  and 10  $\mu\text{m}$  spacing from the LD facet. Average excess coupling loss between a 8-channel LD array and a flat facet single-mode optical fiber array is 1.0 dB, corresponding to an alignment error of 1.8 $\mu\text{m}$ . The coupling loss was 9.2  $\pm$  1.0 dB. The loss was nearly as good as those achieved using active alignment.

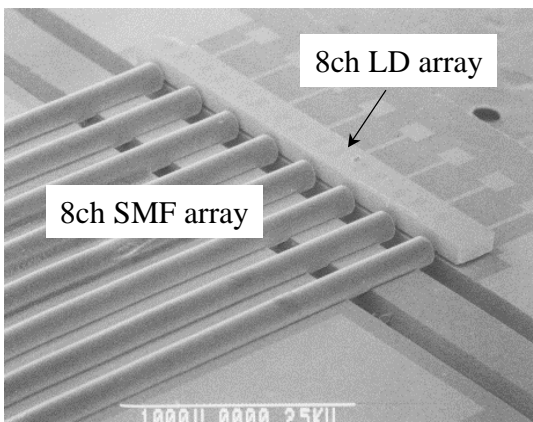


Figure 23 LD array module optical platform.

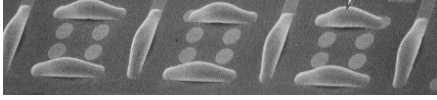


Figure 24 Stripe-type bumps .

C. 4x4 Optical Matrix Switch Module: Figures 25 and 26 show a schematic diagram and a photograph of the hybrid integrated 4x4 optical matrix module (Sasaki, et. al. 1998, Kato, et. al. 1998). Four sets of silica optical waveguide 1:4 splitter, 4:1 combiner and some electrical signal lines were formed on a Si platform. Four 4-channel spot-size converter integrated semiconductor optical amplifier (SOA) gate (Hatakeyama, et. al. 1997) array chips were mounted on the platform by using stripe-type AuSn solder bump flip-chip bonding. The stripe-type bump is the same as one shown in Figure 24. The SOA gates were first put on solder bumps formed on the platform. As the solder bump re-flowed, they were simultaneously self-aligned to their correct position. The positioning accuracy less than  $1\mu\text{m}$  was achieved in both lateral and vertical directions. Two sets of single mode optical fiber (SMF) arrays were assembled in V-grooves fabricated at both ends of the platform. Here, facets of the silica waveguides were formed by using mechanical sawing technique with a dicing blade due to its easiness and low cost capability. This process, however, also cut the electrical wiring patterns connected to optical chips. In order to overcome this problem, printed wiring chips (PWCs) which bridged electrical connection across over such a blade-cut region were employed as shown in Figure 27. The PWCs and SOAs were simultaneously mounted by the solder bump re-flow. The PWC could be charged by some electronics such as driver ICs. The insertion losses at injection current of 50mA were 7.4dB. The coupling loss between an SOA and a silica waveguide was estimated to be about 4.5dB.

## 5.4 Critical Issues

Solder has been widely used for die-attachments in existing optoelectronic products. In addition, most of the aforementioned new modules using solder for precision alignments have been demonstrated in R&D laboratories. As shown in the case study, it is not easy to transfer these new solder technologies from laboratories to manufacturing facilities. Without using mechanical stops, a precise process control of solder volumes is necessary, and external loadings such as gravitational, gas flow, vibration and other forces should be eliminated. The nearly well-aligned solder joints do not have larger self-alignment forces to overcome the effects of these loadings. Using the mechanical stops, however, the interfacial friction forces

among the stops have to be overcome. Misaligned solder joints have large restoring or vertical reaction forces, but they may not be large enough to move the component once the stops make the contacts. Using one mechanical stop for the height control (Lee et al., 1995), the lateral self-alignment should be accomplished before the component touches the standoff. Such a dynamic sequence is a challenge. Using two mechanical stops, the solder self-alignment forces must overcome the friction from either the lateral or the vertical interfacial contact.

As a result, repeatability of the alignments from one module to the other may be a problem. Statistics of self-alignment result with large deviation was frequently reported by Deshmukh et al. (1993), Dautartas et al., 1995, and McGroarty et al., 1993. An example of complete self-aligned optical subassembly shows that the best self-alignment result was 2µm; however, the average was 5µm and the worst was 10µm (Dautartas et al., 1995). More studies are needed to improve the design and manufacturing processes of these modules for a wide application of low-cost, high-performance, high-reliability modules. In particular, four critical issues on solder material, fluxless reflow, design and reliability are to be discussed in the following sections.

**5.4.1 Solder Material and Deposition**

Table 2 lists major solder materials used for optoelectronic packaging. Important solder properties are melting temperature, Young’s modulus, coefficient of thermal expansion, Poisson ratio, fatigue behavior, and creep rate. Indium-based solder has been used for prototyping, but it is not a good material for high-volume manufacturing because its high cost, large creep rate, poor corrosion resistance and high thermomigration rate (Shimizu et al., 1994 and Koopman et al., 1988). In addition, indium is a very efficient dopant and demands careful design and manufacturing control to avoid problems caused by indium diffusion. Pb/Sn-based solder is commonly used in electronic packaging. Its fatigue behavior is well accepted, but its creep may result in µm-level misalignment and degrade the coupling performance. In addition, eutectic solder might form intermetallics with Au. The stoichiometric binary compound is generally very brittle. Early failure may be resulted. Therefore, it may not be appropriated if Au layer is more than 0.25µm (Hinch, 1988). Au/Sn solder are not subject to fatigue or creep rupture during thermal cycling because of its high strength, however, it may transfer the stress to the device and cause cracking in the die.

Table 2. Solder materials used for optoelectronic packaging

Solder alloy	Melt T. (°C)	E	α	γ	Relative fatigue life	Relative creep rate
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63Sn37Pb Eutectic	183	30	21	0.4	10	2
90Pb10Sn	268	20	29	0.4	1	1
95Pb5Sn	310	24	26	0.37	1	0.5
80Au20Sn Eutectic	281	68	14	0.4	poor	N/A
50In50Pb	180	14	27	0.44	3	0.5
100In	157	7	31	0.46	20	Soft
97Sn3Cu	227	41	19	0.33	5	0.01
77.2Sn 20In2.8Ag	175	39	28	0.4	N/A	<0.01

Note:

E: Young's Modules, Unit: GPa.

$\alpha$ : CTE, Unit: ppm/°C.

$\gamma$ : Poisson ratio.

There is a need for a high-fatigue, low-creep solder alloy that is compatible with the electronic manufacturing infrastructure. In addition, the toxicological and legislative issues might result in future restriction in use of Pb/Sn-base solder. As a result, many new lead-free solder alloys are being developed, and some of them may be better than the existing materials for optoelectronic packaging. For example, as shown in the table, a new solder alloy, 97Sn/3Cu, has been developed for lead-free manufacturing for automotive electronics. The creep rate of this material was shown to be 100 times less than that of 90Pb/10Sn (See Figure 25 taken from Pao et al., 1993 and Pao et al., 1995, and Lee N-C, et. al. 1994), and its number of temperature cycles to failure for the configuration tested was 5 times longer than that of 90Pb/10Sn. Another new solder alloy, 77.2Sn20In2.8Ag, has developed as a “drop-in” replacement for eutectic solder. Its creep rate is 2.5 orders of magnitude lower than that of the eutectic solder, which has similar physical characteristics (Lee, N-C, et. al. 1994, Lee, N.C. 1998). The relative creep rate and fatigue life of other solder alloys are compared in the table. The ratios were estimated based on the experimental data in (Shimizu et al., 1994, Pao et al., 1995 and Darveaux et al., 1995). Creep rates and fatigue lives are strongly dependent on not only materials but also microstructures and configurations. These ratios are listed here for qualitative guidance. Nevertheless, it is clearly indicated in the comparison that new solder alloys, e.g. 97Sn/3Cu and 77.2Sn20In2.8Ag, may enhance solder joint performance substantially for optoelectronic packaging. Further studies should be conducted to confirm the expected enhancement and investigate packaging/manufacturing issues associated with the new materials. For examples, the 77.2Sn20In2.8Ag alloy has two drawbacks:

1. The wetting time is about twice as long as that of the eutectic solder at 200°C.

2. The low temperature eutectic point at 118°C, was detected for this alloy. It may define the maximum service temperature of this alloy (Artaki, 1994).

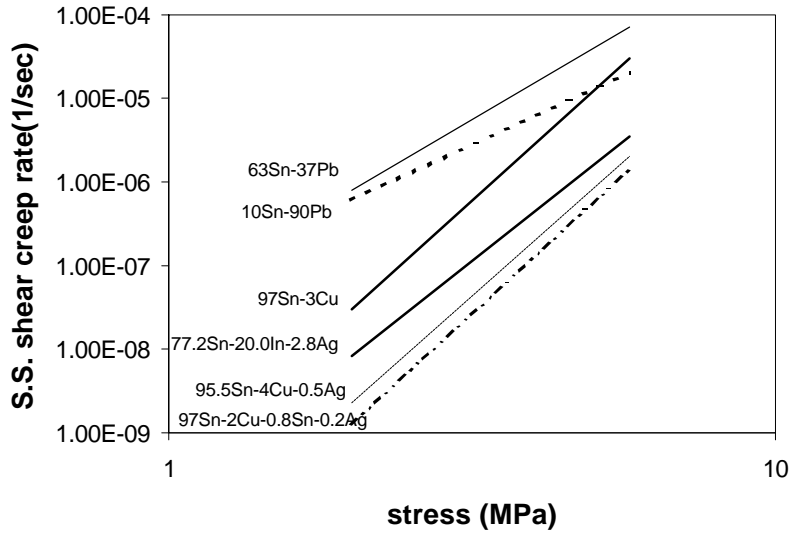


Figure 25: Creep rates of 97Sn/3Cu and other solder alloys.

Solder deposition has been a research focus since IBM first introduced the C4 technology because the evaporation of solder is expensive. Different bumping technologies were developed to reduce cost in microelectronic industry. These technologies are listed in Table 3.

Table 3. Solder bumping methods (Patterson, et. al. 1997, Pittroff, et. al. 1997)

Method	Advantage	Disadvantage
evaporation	<ul style="list-style-type: none"> <li>❖ Clean vacuum process</li> <li>❖ Accurate control of chemical composition</li> <li>❖ Accurate bump volume</li> </ul>	<ul style="list-style-type: none"> <li>❖ Expensive</li> <li>❖ Not suitable for eutectic Pb/Sn</li> </ul>
electroplating	<ul style="list-style-type: none"> <li>❖ Relatively low cost</li> <li>❖ Relatively accurate bump volume</li> </ul>	<ul style="list-style-type: none"> <li>❖ Less accurate control of chemical composition</li> <li>❖ Possible formation of void</li> </ul>
stencil printing	<ul style="list-style-type: none"> <li>❖ Very low cost</li> <li>❖ Compatible with all solder alloy</li> </ul>	<ul style="list-style-type: none"> <li>❖ Less accurate control of solder bump volume</li> </ul>
solder ball bumping	<ul style="list-style-type: none"> <li>❖ Simple, quick, low cost.</li> <li>❖ Suitable for prototyping</li> </ul>	<ul style="list-style-type: none"> <li>❖ Not suitable for production due to slow sequential process</li> </ul>
micropunch	<ul style="list-style-type: none"> <li>❖ Low cost</li> <li>❖ Deposition of large solder volume</li> </ul>	<ul style="list-style-type: none"> <li>❖ Sequential process</li> </ul>
solder jet	<ul style="list-style-type: none"> <li>❖ Capable of using Al as metalization</li> <li>❖ Possible very low cost</li> </ul>	<ul style="list-style-type: none"> <li>❖ Still under development</li> </ul>

It is important to understand that the requirement of bumping for optoelectronic and microelectronic packaging are different in some aspects. In optoelectronic packaging, an accurate control of solder volume is critical so that an accurate alignment can be assured. Therefore, stencil printing of solder is unlikely to be used due to its high bump volume variation

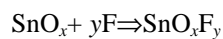
unless such a problem is solved. On the other hand, the high solder volume, which is one of the major challenges for most of the microelectronic packaging, may not be as critical for optical application due to their small sizes. For the solder jet process, liquid solder droplets are ejected from a capillary and impinge the bond pads, just as an ink-jet printer. Deposition of aluminum pad is also demonstrated, which is usually considered as a non-solderable metalization (Hayes, et. al., 1996). It might be a low cost alternative to evaporation, electroplating and micropunch processes.

#### 5.4.2 Solder Reflow

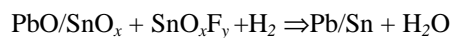
Liquid flux is widely used to remove solder oxides for efficient wetting and self-alignment. The flux residue removal is mandatory and constitutes environment threats (Lin, 1995, Potier et al., 1995 and Frear et al., 1995). More important, the use of liquid flux may contaminate the optically active surface by organic residue (Miller, 1969), and a conventional cleaning method may not be effective for the optoelectronic assembly (Lee and Basavahally, 1994 and Lin, 1995). As a result, different fluxless soldering processes have been developed for soldering optoelectronics modules.

There are two different approaches for the fluxless soldering. The first one involves a precleaning process to remove surface oxide and a reflow process protected from oxidation. For example, PADS (Plasma Assisted Dry Soldering) developed by MCNC uses a microwave reactor (Koopman et. al., 1993 and Koopman et. al., 1996). The following equations explain the PADS process:

##### 1) Plasma Assisted Dry Soldering



##### 2) Hydrogen reflow



In the microwave chamber, an inert, non-flammable, fluorine containing gas such as  $\text{SF}_6$  is disassociated to form atomic fluorine, which is active. The atom fluorine then react with solder oxide and convert oxide to oxyfluoride. This film passivates the solder and has the unique property of breaking up when solder melt, exposing a free solder surface which allow reflow and joining to occurs in absence of flux or reducing gas. Assembly of LED module (Bonda, et. al. 1997) and flat panel display module (Nangalia, et. al., 1997) were demonstrated. A similar approach at ambient pressure was also reported by Potier et al. (1995). In addition, Lee and Wang (1992) reported another method using high vacuum deposition of a gold or copper layer to protect inner layer from oxidation.

The second approach uses reactive gas to remove solder oxides. By definition, the reactive gas is flux because its function is to remove surface oxides in order to enhance solderability. However, it is quite different from the liquid flux. With proper control, the gas leaves little residue without a cleaning process and contamination. Two kinds of reactive gases are commonly used in optoelectronic packaging: forming gas (4-10% H<sub>2</sub> in nitrogen or argon) by Lin et al. (1993), Boudreau et al. (1993), and Brady and Deshmukh (1993) and formic acid vapor (1.5-7% HCOOH in nitrogen) by Deshmukh et al. (1993), Dautartas et al. (1995), Lin (1995) and Brady and Deshmukh (1993).

Figure 26 records self-alignment processes with respect to the use of forming gas (10% H<sub>2</sub> and 90% N<sub>2</sub>) and formic acid vapor at different concentrations (Lin, 1995). The case with the forming gas was conducted at a reflow temperature of 280 °C and assisted by the outgas from a piece of FR-4 printed wiring board. The solder did reflow, but the self-alignment process was very slow. After 200 seconds, the component did not reach the steady state, well-aligned position. Similarly, low-concentration formic acid vapor was not effective. However, when the concentration reached 1.6% or higher, efficient self-alignment was completed within a few seconds. The reflow temperature for the formic acid vapor was only 220 °C. Formic acid vapor resulted in efficient solder self-alignment.

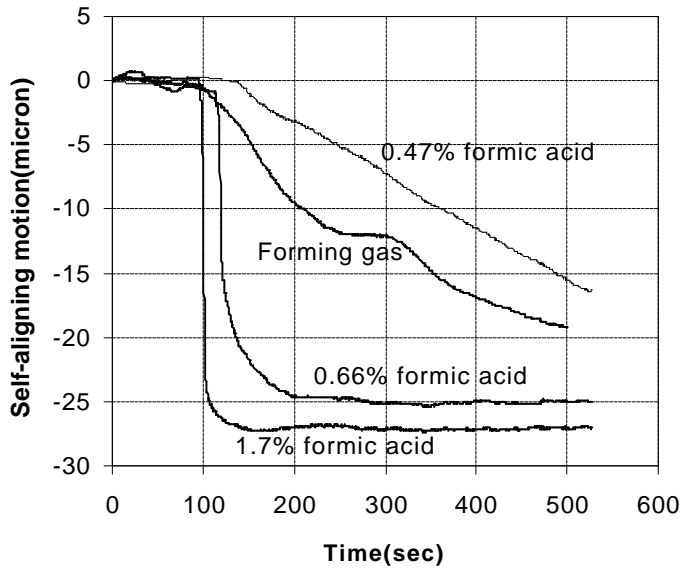


Figure 26: Dynamic self-alignment processes with different reactive gases or concentrations.

Several effects should be further considered when a fluxless soldering process is to be applied for optoelectronic packaging. For example, in order to avoid condensation of the vapor, the assembly temperature should be kept higher than 150 °C during reflow (Lin, 1995). By introducing the gas into the reflow chamber, the flow may move the component and affect the aligning process (Gershovish and Lee, 1994). This gas flow effect is strongly dependent on the flow rate and the

component size. For a chip larger than 5mmx5mm, such a displacement caused by gas flow can be significant. (Su, et. al. 1997)

### **5.4.3 Solder Design**

Experimental result shows that the final alignment accuracy for self-aligned soldering is strongly related to the solder bump parameters such as solder joint diameter and height and the number of joints (Hayashi, 1992). For solder self-alignment, these parameters can be designed for the optimum performance. Modeling studies have been conducted to understand the self-alignment mechanism since the C4 was introduced by IBM (Goldmann, 1969 and Patra and Lee, 1991a). Patra and Lee.(1991a and 1991b) conducted a comprehensive study for the solder joint design. Surface profile was calculated based on the energy minimization principle; the profile was affected by solder pad geometry and size, component weight (or spacer height), surface tension coefficient, solder volume, and misalignment level. The quantitative characterizations could correlate these effects with the height variations that are critical to alignments. The profile and the effects can also be modeled using a public domain software, Surface Evolver (Lin et al., 1995, Martino et al., 1994 and Ju et al., 1993b).

Using the Surface Evolver, Lin et al.(1995) numerically studied the restoring and normal reaction forces as functions of solder joint height, size, volume and misalignment level. A case studied was for a self-aligned module using one mechanical stop for the height control (see Figures 8 and 10). As shown in Figure 28, the vertical reaction force may change from a pulling to a pushing force when the solder volume increases under a given spacer height. There also exists an optimum solder joint volume for the maximum pulling force. With this volume, spatial light modulator shown in Figure 10 was successfully developed by by Lin et al., (1993), Ju et al. (1993a) and Lin (1995). However, it should be noted that the shrinkage of the structural elements during cooling also play a critical role in the gap control. A proper mechanical design considering stresses/strains is needed to assure a good quality assembly (Hareb, 1998).

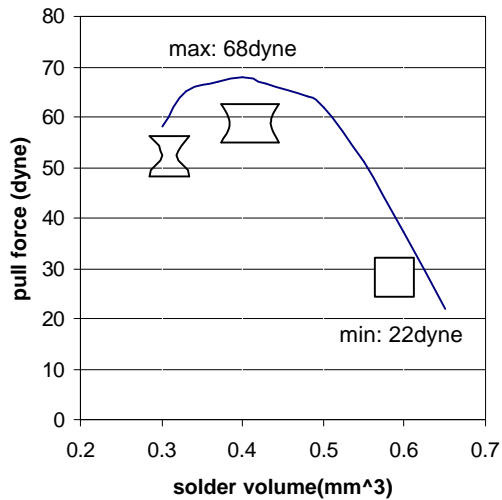


Figure 28: Solder normal reaction force as a function of solder volume.

Figure 29 is a laser-waveguide-fiber module developed by Morozova et. al. (1997). A controlled self-alignment motion was achieved by design for self-alignment. The module contained a laser chip, a tapered polymer waveguide chip and an optical fiber. The laser came out from the LD was coupled to the fiber through the polymer waveguide. The position of the optical fiber was defined by the V-groove. Both laser chip and waveguide were alignment to the glass substrate using self-aligning soldering. The alignment requirements for this module were: 1) the chips should be precisely aligned laterally and vertically, and 2) the axial gap between the LD and waveguide should be precise. As discussed in Section 5.2, such requirements could be achieved using mechanical stop. Unfortunately, the fabrication of mechanical stop was so expensive that the axial gap was chosen to be close to zero. It means that the LS and the waveguide should make a solid contact. For any self-alignment using one mechanical stop, there is a two-axis alignment problem: the chip could get contact with one of the mechanical stop first, then the friction force could hinder the alignment motion in the other direction. In order to achieve an accurate lateral alignment and the solid contact, the alignment motion of the laser chip was controlled. The lateral alignment happened first, followed by the slow axial movement to make the contact. Such a controlled self-alignment sequence was accomplished by using rectangular solder bond pads. As shown in Figure 30a, the solder pads were designed to be  $300\mu\text{m} \times 90\mu\text{m}$ . With such a pad design, the calculated restoring force was much larger in lateral than that in axial for the same misalignment (Figure 30b). As a result, the lateral alignment motion was much faster than the axial motion. The controlled sequence was achieved with an alignment accuracy of  $2\mu\text{m}$  at lateral and a solid contact between the laser chip and the waveguide.

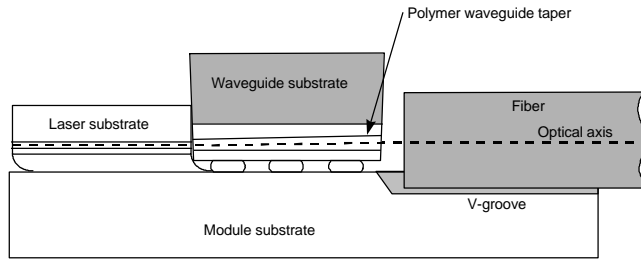


Figure 29: Laser-waveguide-fiber module: controlled self-alignment motion

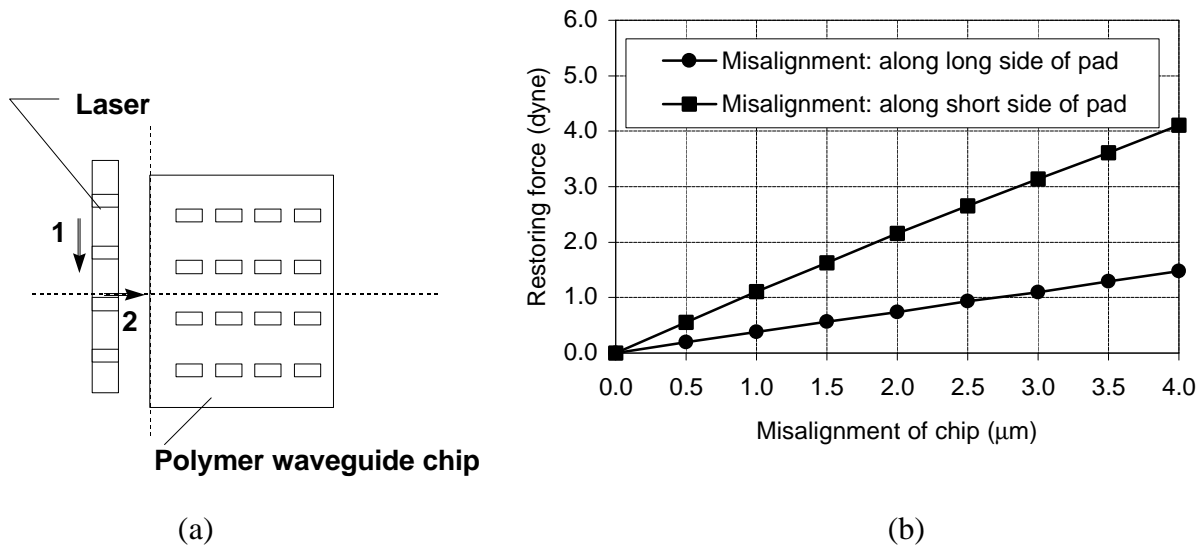


Figure 30: a) design for control self-alignment motion, b) calculated restoring force

Modeling of profiles and self-alignment movement is critical to design solder parameters to reach desirable performance. Number of trial-and-error runs can be reduced. More important, the solder self-alignment can be considered in the trade-off analysis for optoelectronic packaging. Such an analysis considers electrical parasitic capacitance and inductance, thermal resistance, stress/strain, and solder joint reliability. For example, a small solder joint height is desirable for a strong restoring force (Lin et. al., 1995), and it is also preferred to lower thermal resistance and inductance across the solder. However, the small height may result in early fatigue failure. Quantitative analysis of these constraints is necessary to derive an optimum solder design. Among these constraints, solder joint reliability has been rarely considered for optoelectronic packaging although it is a critical factor commonly evaluated for electronics packages. This reliability issue is to be discussed in details in the next section.

#### 5.4.4. Solder reliability

Most of the studies on solder-assembled optoelectronics modules have focused on how to obtain high alignment accuracy rather than on how to maintain the alignment obtained. The long term stability of the alignment accuracy depends heavily on the mechanical integrity of solder joints and their attaching layers.

Solder failure mechanisms are driven by temperature, moisture and voltage. The thermal expansion mismatch between a chip and a substrate could result in stress/strain/fatigue damage of solder connections, optical devices and layers of metallization or dielectrics. Moisture and voltage combined could result in corrosion or metal migration (Lowe and Lyn, 1995). Although a variety of mechanisms may result in cracked solder joints, the major cause of such damage is thermal stress and low cycle, strain-controlled fatigue (Lau and Rice, 1985). Fortunately, for most of optoelectronic modules, the assembly sizes are small, e.g 300  $\mu\text{m}$ , the thermal mismatch is much lower than that for microelectronic. Therefore, the reliability issue has not been a major issue at the moment. However, the chip size is getting larger and larger with high integration levels, reliability assessment should be conducted rigorously.

The following table lists solder-related reliability tests for laser modules (Bellcore, 1993).

Table 3: Solder-related reliability tests for laser modules

<b>Test</b>	<b>Conditions</b>
<i>Mechanical Shock</i>	5 times/axis; 500 G, 1.0msec
<i>Vibration</i>	20G, 20-2,000 Hz; 4 min/cycle, 4cycles/axis
<i>Thermal shock</i>	$\Delta T = 100\text{ }^\circ\text{C}$
<i>Solderability</i>	MIL-STD-883 Method 2003
<i>Acceleration Aging</i>	85 $^\circ\text{C}$ ; rated power; $\geq 5,000$ hrs
<i>High Temperature Storage</i>	max. storage T; $\geq 2,000$ hrs
<i>Low Temperature Storage</i>	min. storage T; $\geq 2,000$ hrs
<i>Temperature Cycling</i>	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$ 400cycles; pass/fail in RT environment 500cycles for information 500cycles; pass/fail in uncontrolled environment 1,000cycles for information
<i>Cyclic Moisture Resistance</i>	
<i>Damp Heat (if using epoxy)</i>	40 $^\circ\text{C}$ /95%RH 56 days; or 85 $^\circ\text{C}$ /85%RH 2,000 hrs

Pass/fail criteria for most of these tests are 10% or 0.5dB maximum change (or less) in coupling efficiency and no obvious change (beyond measurement error) in threshold current. In these tests, solder may affect the reliability through the following mechanical behaviors.

- Stresses/strains: Soldered assembly may experience large temperature variations during solder reflow processes, on/off operations, and environmental changes. In particular, rapid cooling after reflow may result in large thermal stresses/strains in devices, solder joints, substrates and solder-attached metallization and dielectric thin-film layers. The stresses/strains in these elements and at their interfaces are strongly dependent on the temperature variations, material properties, and physical dimensions (Suhir, 1987).

- Creep: Most of solder materials are soft and may creep under stresses. The stresses may be residual thermal stresses resulting from non-uniform shrinkage of different structural elements. Or, they may be applied by external loadings during manufacturing or operations. Creep properties of some solder materials have been reported with very different behaviors. With the same material, the creep properties can be very different when the solder microstructures are changed due to a process change (Schroeder et al., 1994, Pao et al., 1994, McDowell et al., 1994, and Guo and Conrad, 1993). Unfortunately, precise control of solder creep properties is necessary since sub- $\mu\text{m}$  creep movement can degrade the coupling efficiency more than 10%. With quantitatively understanding and control of solder creep, the best approach is to use no-creep Au/Sn solder such as the case study presented in section 5.3. However, for the hard solder, the stresses-induced should be controlled.

- Fatigue: During temperature cycling, cracks are initiated and propagated across the solder joints. The joints' mechanical strength can be substantially weakened and may not be able to maintain the precision alignments obtained. Even worse, the joints may be broken entirely and loss their electrical and mechanical connections. The following two equations can be used to understand the fatigue behavior of solder joints. These equations are widely used to estimate the fatigue life (number of temperature cycles to failure) for a solder joint away from the center of the assembly (Jeannotte et al., 1988). The life is correlated with the shear strain resulting from different expansion movements when temperature changes.

$$\text{Shear strain} = \Delta\gamma = L (\alpha_1 - \alpha_2) \Delta T / h$$

$$\begin{aligned} \text{Fatigue life} &= N_f = 0.5 (\Delta\gamma/0.65)^{-2.26} \\ &= 0.5 (0.65 h / L (\alpha_1 - \alpha_2) \Delta T)^{2.26} \end{aligned}$$

where

$L$  = distance between the solder joint and the neutral point of the assembly

$\alpha_1$  and  $\alpha_2$  = Coefficients of thermal expansion of the component and the substrate

$\Delta T$  = range of the temperature cycles

$h$  = height of the solder joint

Typical length scale ( $L$ ) for electronic components is in the order of 10mm, and that for most of optoelectronic components is in the order of 1mm. The shear strain in an optoelectronic module is small and the fatigue life is high. In addition, the required “fatigue life” is in the range between 500 to 1000 (see Table 3). As a result, this fatigue behavior is not a major concern for the assemblies.

However, the applications of solder-assembled optoelectronic modules expand fast, and their working environment is more and more severe. AT&T is already testing some of its package for telecommunication applications at 0°C-100°C for 5000 cycles (Viera, et. al. 1993). Therefore, three challenging issues related to solder fatigue need to be dealt with: 1) For non-telecommunication applications, there may be a need to increase the number of temperature cycles and the temperature ranges required for the reliability tests. 2) The length scale ( $L$ ) may be increased to the 10 mm level because of large integration of optoelectronic devices. 3) Because the failure may result from coupling loss, the number of cycle to failure for an optoelectronic assembly may be much shorter than the corresponding electronic one of which the failure is corresponding to a broken joint.

To deal with these issues, it is necessary to evaluate material properties discussed in Table 3. In addition, the solder joint should be designed for reliability. The on-going development of different fatigue modeling approaches for microelectronic packages should be modified for optoelectronic packages. Solder reliability is a critical issue needs to be addressed in the near future.

## **5.5 Conclusions**

Soldering technology for optoelectronic packaging has been reviewed. Representative modules have been presented in four categories: solder assembly with no precision self-alignments, and self-aligned solder assembly with no, one or two mechanical steps. The trend is very clear. In addition to die-attachments, soldering technology has been successfully developed for precision alignments with or without using its self-alignment properties.

A case study on the development of a Au/Sn soldering technology has been presented in details. The study considered bumping technique, stripe-type bump bonding and three applications. In addition, four critical packaging issues have been reviewed; they are solder materials, fluxless reflow, design, and reliability. New solder materials may possess high-fatigue, low-creep desirable properties. PADS and formic acid vapor can be used for an effective "fluxless" reflow process. Profile and force modeling tools are important to engineer solder joints for precision alignments. Solder reliability is becoming more and more important, but it has been rarely studied. All these issues require further studies to support the advancement of optoelectronic packaging for low-cost, high-performance and high-reliability modules.

## **5.6 Acknowledgments**

We would like to acknowledge support from the National Science Foundation (MIP-9058409, EEC-9015128, MIP-9400655). We also express our appreciation to Mr. Jackson of IBM, Mr. Haugsjaa of GTE, Mr. Tsunetsugu of NTT, and Mr. Nagano of NEC for providing the referenced sketches and photographs.

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