

# Single Wafer Encapsulation of MEMS Devices

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**Abstract**—Packaging of micro-electro-mechanical systems (MEMS) devices has proven to be costly and complex, and it has been a significant barrier to the commercialization of MEMS. We present a packaging solution applicable to several common MEMS devices, such as inertial sensors and micromechanical resonators. It involves deposition of a 20  $\mu\text{m}$  layer of epi-polysilicon over unreleased devices to act as a sealing cap, release of the encapsulated parts via an HF vapor release process, and a final seal of the parts in 7 mbar (700 Pa) vacuum. Two types of accelerometers, piezoresistive and capacitive sensing, were fabricated. Piezoresistive accelerometers with a footprint smaller than 3  $\text{mm}^2$  had a resolution of 10  $\mu\text{g}/\sqrt{\text{Hz}}$  at 250 Hz. Capacitive accelerometers with a 1  $\text{mm}^2$  footprint had a resolution of 1  $\text{mg}/\sqrt{\text{Hz}}$  over its 5 kHz bandwidth. Resonators with a quality factor as high as 14,000 and resonant frequency from 50 kHz to 10 MHz have also been built. More than 100 capacitive accelerometers and 100 resonators were tested, and greater than 90% of the resonators and accelerometers were functional.

**Index Terms**—Encapsulation, MEMS, piezoresistive accelerometers, resonators, single wafer.

## I. INTRODUCTION

**M**ICRO-ELECTRO-MECHANICAL SYSTEMS (MEMS) packaging is receiving an increasing amount of attention because it is often the most critical barrier to commercialization. Proper packaging of MEMS devices is paramount to their success because MEMS devices are extremely sensitive to environmental conditions (i.e., dust, pressure, moisture). There are three primary methods used for encapsulating MEMS:

- 1) use of an off-the-shelf package and careful handling techniques;
- 2) attachment of a separate lid, usually glass or silicon, on top of a finished part;
- 3) deposition of some sort of encapsulation layer directly on the device wafer.

Several materials and bonding techniques have been used when attaching a separate lid. Glass wafers have been anodically bonded to silicon to encapsulate MEMS yaw rate sensors [1]. Thermocompression bonding has been used to bond silicon

to glass or gold [2]. Also, intermediate layers of PSG or Indium solder have been used to bond glass wafers at ambient pressure [3]. In order to avoid the deleterious effects high temperature bonding can have on microelectronics, localized polysilicon microheaters have been implemented to focus the heat on the desired bonding area [2]–[5]. A thorough review of localized heating and bonding processes was written by Lin [6].

Of the wafer encapsulation techniques where a layer is deposited on the device wafer to provide encapsulation, two approaches can be seen. One method is to deposit a sacrificial layer on top of the device layer, deposit the encapsulation layer, release the structure by etching away the sacrificial layer via access holes in the encapsulation layer, and reseal these access holes [7]–[14]. The other method is similar except that rather than using access holes to etch away the sacrificial layer, a thin membrane which is permeable to the etch chemistry is used [15], [16].

We have chosen the method of depositing an encapsulation layer at the wafer-scale for several reasons.

- 1) Single wafer packaging allows for a smaller footprint for a packaged device because bond rings are avoided.
- 2) Potential cost savings exist with a single wafer approach.
- 3) Open silicon areas allow for the possibility of integration with CMOS, where the MEMS are fabricated and encapsulated first, and the CMOS is fabricated afterward in the open areas of single crystal silicon adjacent to the MEMS.

This packaging technique is versatile and can be extended to any device that does not need direct physical contact with the ambient (i.e., accelerometers, yaw rate sensors, RF MEMS resonators and filters).

A unique feature of our method of single-wafer encapsulation is the durability of the encapsulation. Our process uses an encapsulation layer that is, at 20  $\mu\text{m}$ , thicker than the previous works discussed. This allows devices made with our process to withstand standard back-end processes, such as wafer dicing, wire bonding and high pressure injection molding of plastic, a common process used for making IC packages. This is the first demonstration of this type of single wafer encapsulation withstanding these back-end processes. The ability to withstand standard back-end processes obviates the need for the complex, expensive, and potentially yield reducing specialty packaging techniques that are prevalent among MEMS devices, such as a the custom dicing technique patented by Analog Devices that was designed to protect released MEMS structures [17].

The feasibility of this thick encapsulation technique was demonstrated when packages that did not contain devices were fabricated to analyze the robustness of the encapsulation layer [8]. In this paper, we describe the first working devices that have been fabricated using this packaging method. In order

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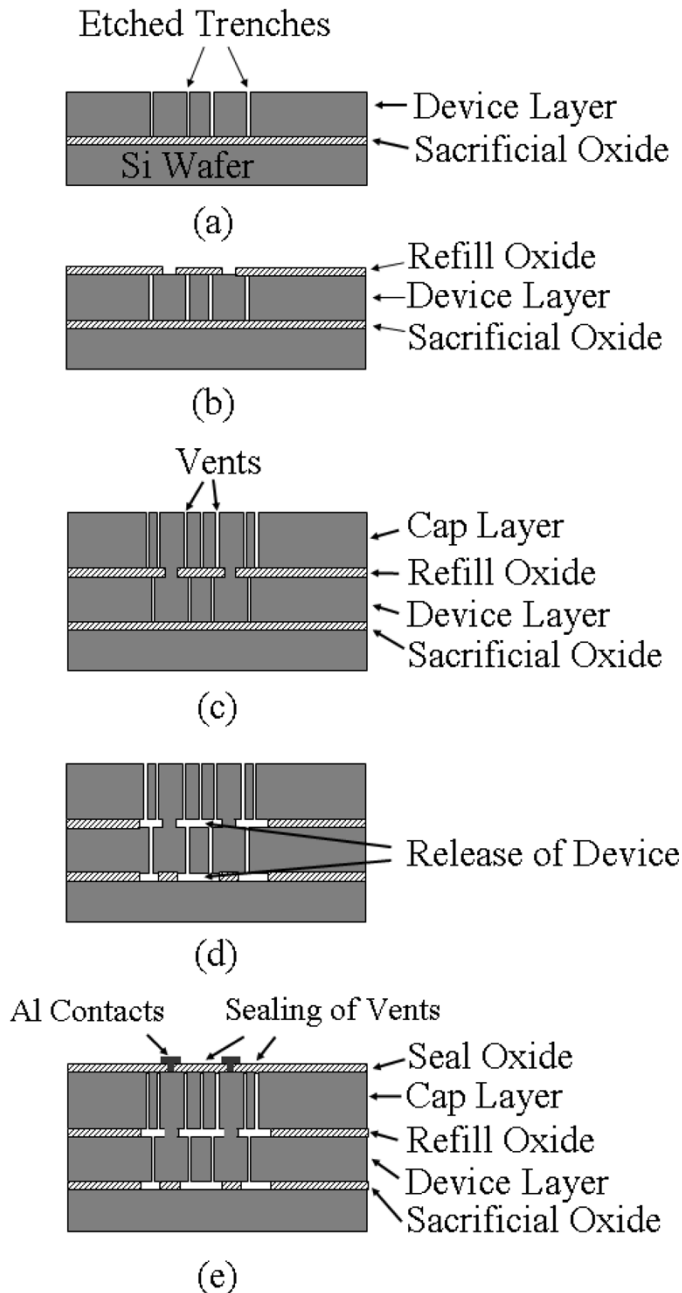


Fig. 1. Cross section drawing of encapsulation process. (a) Etching of device structure. (b) Sealing of trenches with sacrificial oxide and etching of oxide for electrical contact. (c) Etching of cap layer. (d) HF vapor release. (e) Oxide vacuum sealing and deposition of aluminum.

to demonstrate the versatility of this packaging concept, we have encapsulated two types of MEMS devices, accelerometers and resonators. Accelerometers are important MEMS devices because of their relative maturity and common use in commercial automotive and navigational applications [18]. MEMS resonators are a less mature technology from a commercial standpoint, but they show great promise for communications applications [19].

## II. CONCEPT

We demonstrate a novel packaging concept which makes use of a sacrificial spacer oxide layer and a thick layer of deposited

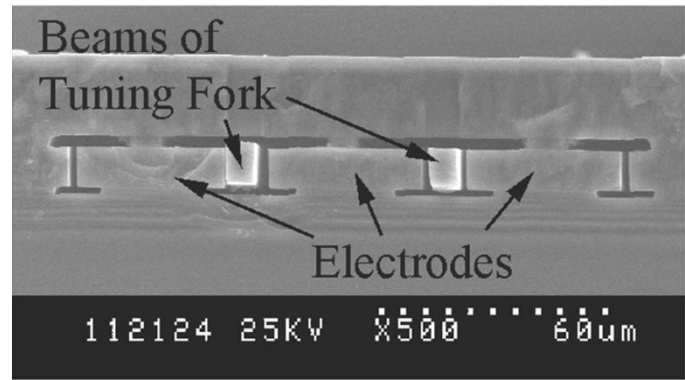


Fig. 2. SEM cross section of encapsulated resonator.

silicon to encapsulate our MEMS devices. The cap layer and device layer are grown in a conventional epitaxial chemical vapor deposition (CVD) reactor. The devices are released with a vapor phase Hydrofluoric Acid (HF) process, eliminating both the problem of stiction and the necessity of a critical point dry (CPD) process. The electrical contacts are routed through the highly conductive encapsulation (“cap”) layer. The finished wafer looks like a plain silicon wafer with bond pads, while the devices are safely buried underneath.

One important feature of this process is that exposed field areas of single crystal silicon will remain single crystal when silicon is deposited on them in our process. This allows the option of fabricating CMOS control circuitry adjacent to the MEMS devices on the same wafer, such that one would have integration of MEMS and CMOS where the MEMS are fabricated first, and the CMOS is fabricated afterward. The MEMS-first integration approach alleviates thermal budget concerns that MEMS would cause if the MEMS were fabricated after the CMOS.

The durability of the cap is critical, as it allows our parts to withstand conventional back-end processing, such as dicing and wire bonding. The cap thickness and the area it spans unsupported are important quantities that define the durability. A thorough analysis of both have been previously published [8].

## III. FABRICATION

The fabrication process begins by growing thermal  $\text{SiO}_2$  as a sacrificial layer, etching away  $\text{SiO}_2$  in places where a substrate contact or single crystal silicon is desired, and depositing the device layer silicon. An alternative to these steps is the use of an SOI wafer. The active structure is etched into the silicon device layer using an anisotropic plasma etch process, as shown in Fig. 1(a). For piezoresistive accelerometers, an implant occurs to define the resistors that sense deflection [20]. At this point, rather than release the devices in HF acid, we cover them with a low pressure chemical vapor deposition (LPCVD) oxide. The oxide seals over the etched trenches, depositing only a minimal amount of oxide down the sidewalls of the trenches.

Openings are etched into the oxide to allow electrical contact to the structure, shown in Fig. 1(b). A layer of silicon, the encapsulation layer ( $>20 \mu\text{m}$  thick), is deposited. In our case, Dichlorosilane at 1080 C was used, giving a deposition rate of  $1.4 \mu\text{m}/\text{min}$ . The encapsulation layer is planarized via chemical mechanical polishing (CMP). Trenches are etched through

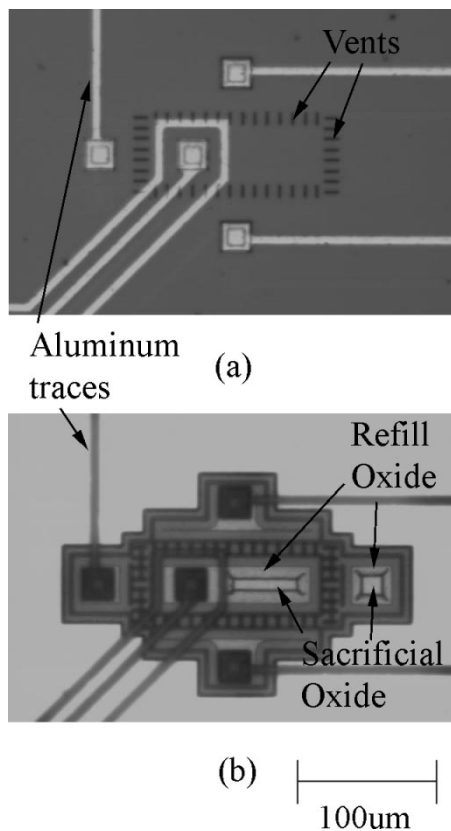


Fig. 3. Optical micrographs of a doubly clamped tuning fork. (a) Top view of encapsulation. (b) View through cap to encapsulated tuning fork using infrared camera and backside illumination.

the cap layer, shown in Fig. 1(c), again using anisotropic plasma etching, for two reasons:

- 1) access to both layers of sacrificial oxide for HF vapor etching;
- 2) isolation of the conductive paths running from the functional layer through the cap.

If the cap layer were not etched to isolate contact areas, then all of the contacts would be shorted together through the conductive cap. Fig. 1(d) shows the release of devices by a timed etch ( $\sim 1$  h) using HF acid in the vapor phase. A layer of LPCVD oxide is deposited which seals over the trenches in the cap layer. Since the oxide deposition furnace is under vacuum, the parts are also under vacuum when sealed. After the sealing oxide is deposited, it is etched to allow electrical contact to the cap surface, which in turn provides electrical contact to the buried structures. Aluminum is deposited and etched as the final step in the process, which is shown in Fig. 1(e). As a side note, one potential drawback to the use of an oxide is its permeability to the ambient gases, which could cause vacuum degradation over time. There are several possible adjustments that can be made to the process to extend the vacuum life, including the deposition of a nitride or metal layer on top of the oxide seal location.

A cross section SEM of a real device can be seen in Fig. 2. Also, images of a packaged resonator structure, a top view in the visible spectrum and the same view illuminated from beneath and viewed with an infrared camera are shown in Fig. 3(a) and (b), respectively.

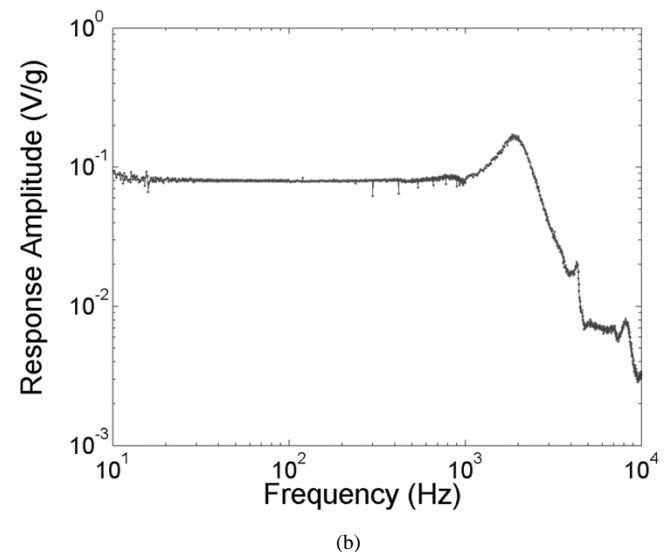
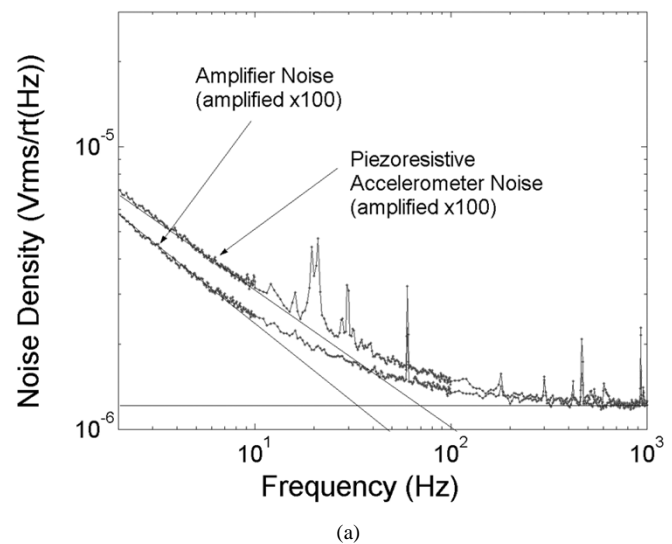


Fig. 4. Data for encapsulated piezoresistive accelerometer using a half bridge measurement with  $100 \times$  signal amplification. (a) Noise spectrum showing accelerometer noise and amplifier baseline noise. (b) Frequency response.

#### IV. RESULTS

Piezoresistive accelerometers, capacitive accelerometers and capacitively actuated resonators were built using this new packaging method. Capacitive accelerometers with a footprint of  $1 \text{ mm}^2$  and resolution of  $1 \text{ mg}/\sqrt{\text{Hz}}$  and piezoresistive accelerometers with a footprint of less than  $3 \text{ mm}^2$  and resolution of  $10 \text{ } \mu\text{g}/\sqrt{\text{Hz}}$  were fabricated. The piezoresistive accelerometer consists of a pie-shaped mass that is connected to a thin flexure which is connected to an anchor at the other end [20]. The mass deflects in-plane when acceleration occurs, causing the flexure to bend. This bending can be sensed by a change in resistance on each side of the flexure as shown in Fig. 8(a). Fig. 4(a) shows the noise spectrum of a piezoresistive accelerometer along with the baseline noise of its amplifier, and Fig. 4(b) shows the frequency response of this accelerometer.

The resonators are doubly-clamped tuning forks, with each resonator consisting of two beams that are anchored at both ends, as can be seen in Fig. 5. The beams are coupled through

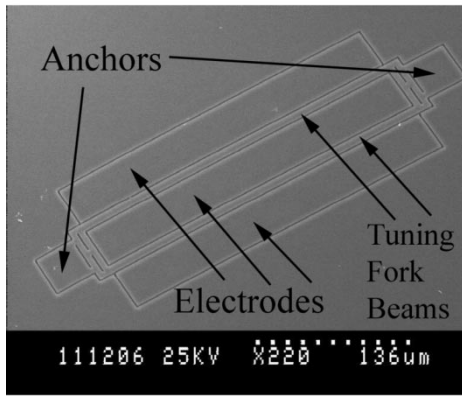


Fig. 5. SEM top view of a doubly-clamped tuning fork before encapsulation.

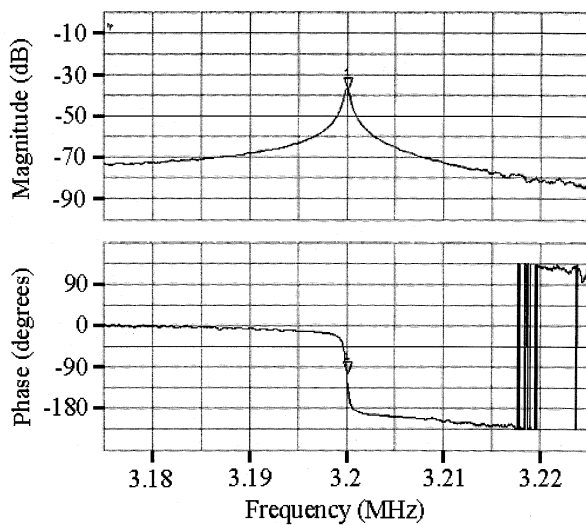


Fig. 6. Gain-Phase plot for 3.2 MHz encapsulated resonator.

the anchors and actuated  $180^\circ$  out-of-phase, ideally resulting in zero net force on the substrate. They are capacitively actuated by electrodes outside the beam, and the output signal is detected by a single center electrode.

Resonators were designed to have resonant frequencies ranging from 50 kHz to 10 MHz, with the quality factor of encapsulated parts reaching higher than 14 000. Each  $1 \text{ mm}^2$  die contains two resonators. A typical Gain-Phase plot of a tuning fork in resonance is given in Fig. 6.

Finished wafers yielded greater than 90% working resonators and capacitive accelerometers with more than 100 of each device tested. Not enough of the piezoresistive accelerometers were tested to provide a reliable value for yield. Virtually all of the device failures resulted from scratches in the contact metal. The pressure inside the cavity was determined to be 7 mBar (700 Pa). The pressure was found by matching the quality factor of encapsulated resonators to the quality factor of resonators whose encapsulation seal had been intentionally removed and were then measured in a pressure controlled chamber. Fig. 7 shows a changing quality factor with pressure. Quality factor follows damping theory [21] down to a critical point where pressure seems to be the limiting mechanism, and thermoelastic dissipation becomes dominant [22].

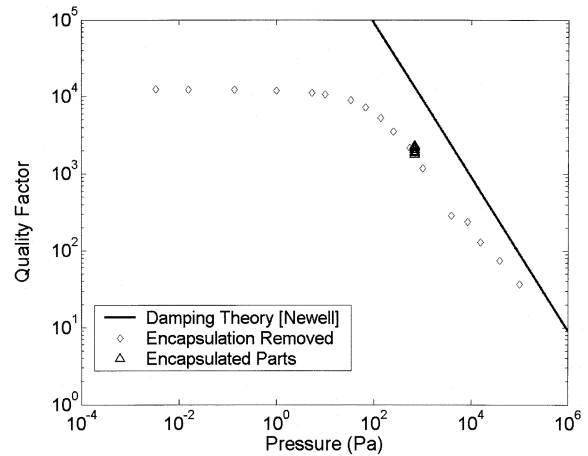
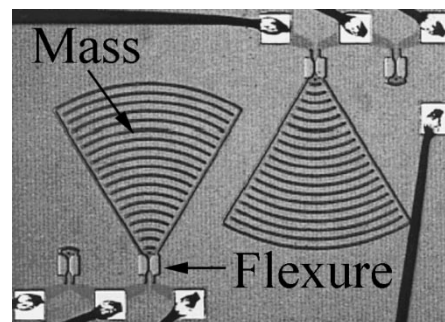
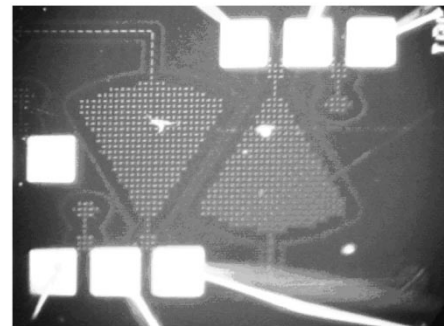


Fig. 7. Quality factor versus pressure plot for 850 kHz resonator. Data points of encapsulated resonator quality factor and corresponding pressure shown.



(a)



(b) 500μm

Fig. 8. Top view of a piezoresistive accelerometer. (a) Without encapsulation. (b) With encapsulation.

The encapsulation was robust enough to handle standard back-end processing. Finished wafers were probed, diced in a wafer saw, epoxied into packages and wire bonded with no loss in yield. An example of this can be seen in Fig. 8, where two piezoresistive accelerometers are shown, one before the encapsulation process was developed, the other being one of our most recent encapsulated devices. It is important to note that the scratches and particles on the encapsulated device would have certainly rendered its unencapsulated counterpart useless.

However, the encapsulated device still worked perfectly despite its rough handling.

## V. CONCLUSION

A novel single-wafer packaging method has been presented that is useful for the prevalent class of sensors and actuators that does not need direct physical or optical contact with the environment, including micromechanical resonators and filters, accelerometers, and yaw rate sensors. Resonators and accelerometers were shown to work within this packaging method, with finished parts withstanding standard back-end processing without harm. The process allows for a MEMS-first CMOS integration approach, where the CMOS would be deposited beside the MEMS devices in single crystal silicon.

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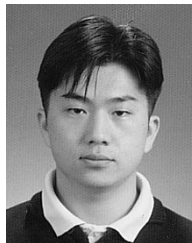
## REFERENCES

- [1] M. Lutz, W. Golderer, J. Gerstenmeier, J. Marek, B. Maihofer, S. Mahler, H. Munzel, and U. Bischof, "A precision yaw rate sensor in silicon micromachining," in *Proc. Int. Conf. Solid State Sensors Actuators (TRANSDUCERS'97)*, vol. 2, 1997, pp. 847–850.
- [2] Y. T. Cheng, L. Lin, and K. Najafi, "Localized silicon fusion and eutectic bonding for MEMS fabrication and packaging," *J. Microelectromech. Syst.*, vol. 9, pp. 3–8, 2000.
- [3] —, "Localized bonding with PSG or indium solder as intermediate layer," in *Proc. 12th IEEE Int. Conf. Micro Electro Mech. Syst.*, 1999, pp. 285–289.
- [4] Y.-T. Cheng, W.-T. Hsu, K. Najafi, C. T.-C. Nguyen, and L. Lin, "Vacuum packaging technology using localized aluminum/silicon-to-glass bonding," *J. Microelectromech. Syst.*, vol. 11, pp. 556–565, 2002.
- [5] Y.-T. L. Cheng and K. Najafi, "A hermetic glass-silicon package formed using localized aluminum/silicon-glass bonding," *J. Microelectromech. Syst.*, vol. 10, pp. 392–399, 2001.
- [6] L. Lin, "MEMS post-packaging by localized heating and bonding," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 608–616, Nov. 2000.
- [7] W.-T. Park, R. N. Candler, S. Kronmueller, M. Lutz, A. Partridge, G. Yama, and T. W. Kenny, "Wafer-Scale film encapsulation of micro-machined accelerometers," in *Proc. Transducers'03*, vol. 2, 2003, pp. 1903–1906.
- [8] A. Partridge, A. E. Rice, T. W. Kenny, and M. Lutz, "New thin film epitaxial polysilicon encapsulation for piezoresistive accelerometers," in *Proc. 14th IEEE Int. Conf. Micro Electro Mech. Syst. (MEMS'01)*, 2001, pp. 54–59.
- [9] C. M. Mastrangelo and R. S. Muller, "Vacuum-sealed silicon micro-machined incandescent light source," in *Proc. Int. Electron Devices Meeting*, 1989, pp. 503–506.
- [10] C. H. Mastrangelo, J. H.-J. Yeh, and R. S. Muller, "Electrical and optical characteristics of vacuum-sealed polysilicon microlamps," *IEEE Trans. Electron Devices*, vol. 39, pp. 1363–1375, June 1992.
- [11] J. D. Zook, W. Herb, A. Yongchul, and H. Guckel, "Polysilicon sealed vacuum cavities for microelectromechanical systems," *J. Vac. Sci. Technol. A*, pp. 2286–2294, 1999.
- [12] M. Bartek, J. A. Foerster, and R. F. Wolfenbuttel, "Vacuum sealing of microvacuities using metal evaporation," *Sensors Actuators A*, vol. 61, pp. 364–368, 1997.
- [13] K. Ikeda, H. Kuwayama, T. Kobayashi, T. Watanabe, T. Nishikawa, T. Yoshida, and K. Harada, "Three-Dimensional micromachining of silicon pressure sensor integrating resonant strain gauge on diaphragm," *Sensors Actuators A*, vol. A21-A23, pp. 1007–1010, 1990.
- [14] H. Guckel, J. J. Sniogowski, T. R. Christenson, and F. Raissi, "The application of fine-grained, tensile polysilicon to mechanically resonant transducers," *Sensors Actuators A*, vol. A21-A23, pp. 346–351, 1990.
- [15] T. Tsuchiya, Y. Kageyama, H. Funabashi, and J. Sakata, "Polysilicon vibrating gyroscope vacuum-encapsulated in an on-chip micro chamber," *Sensors Actuators A*, vol. 90, pp. 49–55, 2001.
- [16] K. S. Leboutz, A. Mazaheri, R. T. Howe, and A. P. Pisano, "Vacuum encapsulation of resonant devices using permeable polysilicon," in *Proc. 12th IEEE Int. Conf. Micro Electro Mech. Syst. (MEMS'99)*, 1999, pp. 470–475.
- [17] C. Roberts, L. Long, and P. Ruggerio, "Method for separating circuit dies from a wafer," 5 362 681, 1994.
- [18] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proc. IEEE*, vol. 86, pp. 1640–1659, 1998.
- [19] C. T.-C. Nguyen, "RF MEMS for wireless applications," in *Proc. Device Res. Conf.*, 2002, pp. 9–12.
- [20] A. Partridge, J. K. Reynolds, B. W. Chui, E. M. Chow, A. M. Fitzgerald, L. Zhang, N. I. Maluf, and T. W. Kenny, "A high-performance planar piezoresistive accelerometer," *J. Microelectromech. Syst.*, vol. 9, pp. 58–66, 2000.
- [21] W. E. Newell, "Miniaturization of tuning forks," *Science*, pp. 1320–1326, 1968.
- [22] R. N. Candler, H. Li, M. Lutz, W.-T. Park, A. Partridge, G. Yama, and T. W. Kenny, "Investigation of energy loss mechanisms in micromechanical resonators," in *Proc. Transducers'03*, vol. 1, 2003, pp. 332–335.



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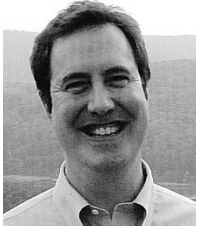
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